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A number of analog circuit modules are assembled on a single integrated circuit chip with the ability of the user to program, through pins of the circuit, certain functions and operational parameters of the individual modules, and to interconnect the modules in a specified way in order to form a desired analog system on the single circuit. Support and diagnostic modules are also included. The individual modules are configured, and those forming the analog circuit interconnected together, by configuration data that is loaded into a series connection of configuration registers. Individual ones of the configuration registers are separately addressable, however. The interface characteristics of the individual signal modules are made such that they may be connected together in a number of different combinations without affecting operation of the individual modules.

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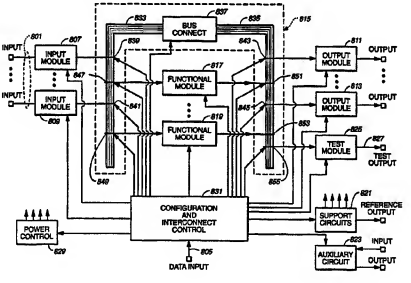

(57) Abstract

A number of analog circuit modules are assembled on a single integrated circuit chip with the ability of the user to program, through pins of the circuit, certain functions and operational parameters of the individual modules, and to interconnect the modules in a specified way in order to form a desired analog system on the single circuit. Support and diagnostic modules are also included. The individual modules are configured, and those forming the analog circuit interconnected together, by configuration data that is loaded into a series connection of configuration registers. Individual ones of the configuration registers are separately addressable, however. The interface characteristics of the individual signal modules are made such that they may be connected together in a number of different combinations without affecting operation of the individual modules.

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INTEGRATED CIRCUIT HAVING PROGRAMMABLE ANALOG MODULES WITH CONFIGURABLE INTERCONNECTS BETWEEN THEM

BACKGROUND OF THE INVENTION

This invention relates generally to integrated circuit chip products whose functions and interconnections are programmable.

A widely used type of digital integrated circuit contains a large number of basic digital circuit modules which are configurable by a user. A digital system is formed by application of configuration signals to the circuit product. The circuit modules include standard digital circuit building blocks, such as AND-gates, OR-gates, inverters, flip-flops, and the like. Inputs and outputs of these basic digital building blocks are connectable together by switches and interconnecting lines that are formed as part of the circuit. This type of product is commercially known as a field programmable gate array (FPGA).

In one form, the configuration switches are semiconductor pass gates whose states are controlled by the contents of registers that are also provided on the chip, the registers being loaded with the configuration data each time the system in which the chip is a part is powered up or reset. This configuration data is developed, and can be reconfigured, by the end user.

Another popular technology that is not reconfigurable uses anti-fuses as part of the integrated circuit. These connection devices are selectively blown by application of signals to the circuit by the end user to interconnect the digital modules in a desired manner.

The anti-fuses are used in place of the pass gates mentioned in the previous paragraph.

Such configurable digital circuits allow the end user to implement a custom digital system design without having to have a dedicated integrated circuit or gate array designed and manufactured for a single purpose. This permits systems to be built where the volume of production is insufficient to justify the considerable cost of a special single purpose integrated circuit or gate array. Further, in the case of those types of circuits which are reconfigurable, the end user can test a digital system design and alter interconnections between digital logic blocks, as required, before the specific interconnects to be used in the system are finalized.

The extension of this technique to the inclusion of analog circuit modules with configurable digital logic has been contemplated. Such analog circuit modules include amplifiers, comparators, oscillators, voltage and current reference sources, and the like, which can both be configured to some extent and interconnected by the end user from outside the circuit chip to implement a specific analog circuit.

However, the design of such an array of interconnectable analog modules involves different considerations than in the design of digital logic arrays. In the digital domain, the most complex circuits are formed of only a few types of primitives and the communication of binary signals between such primitives makes it relatively easy to group them in modules that can be interconnected together in an almost limitless number of ways to build a complete digital system. Because of limitations in analog circuits and signals which are not

present in the digital domain, such flexibility has not heretofore been provided in the analog domain.

Therefore, it is a principal object of the present invention to provide a user configurable integrated circuit having a plurality of analog modules that can be used with the same convenience and flexibility as existing FPGAs.

It is another object of the present invention to provide various specific improvements in analog circuit techniques for use in such an integrated circuit.

It is also an object of the present invention to provide a plurality of analog modules, on an integrated circuit chip, that are easily and conveniently configurable by an end user.

It is a further object of the present invention to provide improved configuration and other techniques that may be applied to a wide variety of types of integrated circuits.

SUMMARY OF THE INVENTION

Briefly and generally, a programmable analog system is provided on a single integrated circuit chip having signal input, signal output and configuration data input pins, among others. Signal input modules and signal output modules allow for connection of the input and output pins, respectively, to a configurable interconnection network. The input modules can also include programmable circuit functions, such as buffering, filtering, switching, and other signal conversion functions that enable the chip to be adapted for use in a wide variety of types of analog systems. Similarly, the output modules can provide various selectable functions including buffers, switching circuits, comparators, and

the like. If the circuit chip is designed to interface directly with a digital system, the input module can include a digital-to-analog converter, and the output module can include an analog-to-digital converter. There is no need, however, for any other digital signal processing on the chip, all the signals being otherwise conveyed and processed in analog form.

A plurality of functional analog circuit modules are connected to each other and to the input and output modules through the configurable interconnection network. A wide variety of analog circuit functions can be included in individual functional modules, such as amplifiers, comparators, adder/subtractors, filters, rectifiers, and other normally used analog circuits. An individual functional module preferably includes a more complex circuit that is programmable by the user to perform a selected one of two or more such functions. Operating parameters of the various modules, when set to perform a certain function, are also programmable. Examples of such parameters include the gain of an amplifier, the bandpass characteristics of a filter, the threshold characteristics of a comparator, the level of hysteresis of a comparator, and similar known analog circuit parameters.

It is also desirable to provide one or more support modules not directly connectable in the analog signal path but which provide support to other modules or configuration circuitry. One example is a bias voltage or current generator whose voltage, current or other characteristic of its output is programmable. Another is a clock oscillator having programmable frequency clock signals.

In order to program all the modules in the system and interconnect the input, functional and output

modules together to form a customized operable analog circuit between the input and output pins, a digital configuration circuit is provided. In a preferred form, the configuration circuit includes a plurality of series connected registers which are serially loaded with configuration data from the configuration data input pins. Specific fields of the configuration data registers are connected to program operation of individual modules and to interconnect the input, functional and output modules. Although serially connected, the registers are individually addressable in order to allow the function of one module or a specific connection between modules to be rapidly reprogrammed or reconfigured at a time. Further, duplicate registers may be included, as part of the serial chain, in some or all the modules in order to allow a rapid change from one configured function, operating parameter or interconnection to another. This flexibility to dynamically change attributes of the circuit while the circuit is operating is not available with usual analog circuits. Configuration data to be loaded into these registers upon initialization of the circuit chip may be stored in non-volatile memory provided on the chip in a manner that any dynamic changes made during operation do not affect the contents of the memory. These improved digital configuration techniques are not limited to use in configurable analog circuit module integrated circuit chips but also have application in FPGAs and any other circuit wherein flexibility and ease in its programmability is desired.

In a specific form, the module interconnection circuits include a bus having a number of signal paths with one of the internal input or output of the individual modules being permanently connected to a unique one of the

internal bus signal paths. The other of the internal input or output of the individual modules is then selectively connected to a designated number or all of the bus signal paths. Selective connection of an individual module to the bus is made, in one form, by a transistor switching circuit operated in response to a designated field of the configuration data stored in one of the serially connected registers.

This internal module interconnection technique allows a test probe feature to be easily included as part of the chip. A test probe module may be provided to allow the user to connect any one or more of the bus signal paths to a limited number of pins for the purpose of monitoring analog signals in those paths. The particular bus signal path(s) connected to the outside is selected by configuration data directed loaded into a series connected configuration register of the test probe module.

The functional modules, and to some extent the input and output modules, may be made to operate with either voltage or current analog signals. The best type of circuit technique to be employed within the modules depends upon the frequency range, bandwidth, voltage swing, noise tolerance and other characteristics of signals with which the circuit chip is expected to be used. In either case, the internal input and output interfaces of the interconnectable modules are constructed so that their operation and effect on the analog signals are substantially independent of which other modules are interconnected together and any variations of impedance or other characteristics between specific module interconnections. The modules are constructed to be interconnected together in a wide variety of different combinations according to the desired overall circuit

intended to be configured, all without the quality of the analog signal or operation of the individual modules being adversely affected by any of a large number of different possible connection paths being utilized between the input, functional and output modules.

In the case where the signals are carried within the individual modules by a varying voltage (voltage or charge mode) and communicate voltage varying signals between modules, the input impedance of the individual modules is made to be very high, and the output impedance is made to be very low. In the case where the modules carry signals as current variations (current mode) and communicate current varying signals between modules, the input impedance of the individual modules is made to be very low and its output impedance made to be very high. It is preferable, for maximum flexibility of interconnections, that these relative impedance characteristics be maintained for each module's input and/or output that is connected to the interconnection network between them.

The various aspects of the present invention, individually and in combination, provide an integrated circuit chip which processes analog signals in a way that may be easily and rapidly configured and programmed by the user. The user can select from a wide variety of individual module circuit options without creating any undesired side effects from the selection of any one option. The user can also interconnect the modules in any of a large number of permitted combinations without affecting operation of the modules or causing harm to the circuit chip. It is preferred to physically limit the individual module programming options and the interconnect possibilities to only those which form stable operating

circuit modules and systems. It has been found preferable to do this, rather than allow potentially inoperable configurations which the user, and/or a programming software tool, must know to avoid. The chip product can thus be used by persons who do not possess expert analog circuit design skills. Any programming software tool which may be used to assist in the chip programming is thus also simplified.

The foregoing outlines only the highlights of some of the principal features of the present invention. Other features, objects and advantages of various aspects of the present invention are contained in a detailed description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A, 1B and 1C are diagrams which show different examples of a system included on an integrated circuit chip which implement various aspects of the present invention;

Figure 2 is a circuit diagram of a portion of the system of Figure 1C;

Figure 3A illustrates a format of command and configuration data that is used in the system of Figure 1C and circuit of Figure 2;

Figure 3B shows an example configuration data file that is loaded into the circuit chip of Figures 1C and 2;

Figure 4 illustrates a general structure of an input module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 5 illustrates a general structure of a functional module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 6 illustrates a general structure of an output module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 7 illustrates a general structure of the test probe module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 8 is a circuit of a cross-point switch used in the modules of Figures 5-7;

Figure 9 illustrates a general structure of the internal bias generator module a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 10 illustrates a general structure of an auxiliary module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 11A illustrates use of several circuit chips of the type shown in Figure 1C;

Figure 11B illustrates a specific application of the circuit chip shown in Figure 1C;

Figure 12 generally illustrates the impedance interface characteristics between voltage mode types of modules when employed in a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figures 13a, 13b, 13c and 13d illustrate basic analog voltage mode cells that may be employed in a functional module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 14 is a schematic diagram of a voltage mode cell for use in a functional module of a system of any of Figures 1A-1C, with particular reference to the

system of Figure 1C, wherein any of the basic analog functions of Figures 13a-d are selectable by appropriate configuration data;

Figure 15 illustrates another voltage mode cell for use in a functional module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C, which allows its function to be programmed by configuration data;

Figure 16 is a schematic diagram illustrating one form of a configurable center tap resistor;

Figure 17a, 17b and 17c illustrate alternative signal conversions which may be employed in an input module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 18a, 18b and 18c illustrate alternative signal conversions which may be employed in an output module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 19 illustrates generally the impedance interface characteristics of current mode types of modules when employed in a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 20 illustrates the input/output connections of a current amplifier usable in functional modules of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 21 is a schematic diagram of an example voltage-to-current conversion cell used in an input module of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figures 22a and 22b are schematic diagrams of alternative current-to-voltage conversion cells which can be employed in the output modules of a system of any of

Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 23 illustrates generally the impedance characteristics of charge mode types of cells when used in the functional module of Figure 5 as part of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 24 is a schematic diagram of an example programmable charge mode cell of the functional module of Figure 5 as used in a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 25 is a timing diagram illustrating operation of the circuit of Figure 24;

Figure 26 is a block diagram that illustrates the phase relationship between signals of adjacent charge mode functional modules;

Figure 27 is a block diagram that illustrates a way of interconnecting charge mode functional modules of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 28 is an example charge mode cell used in the output module of Figure 6 when employed in a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 29 is an example charge mode input cell for use in the input module of Figure 4 in of a system of any of Figures 1A-1C, with particular reference to the system of Figure 1C;

Figure 30 is a schematic diagram of a modification of a portion of the system of Figure 1 which allows storing and selective use of multiple sets of configuration data;

Figure 31 shows details of a portion of the circuit shown in Figure 30;

Figure 32 illustrates a variation of the test probe circuit of Figure 7;

Figure 33 shows use of a configurable analog circuit chip of the present invention as part of a complete system;

Figure 34 illustrates a specific configuration of the configurable analog circuit chip of the present invention;

Figure 35 is one specific layout of the circuit chip of the present invention; and

Figure 36 is another specific layout of the circuit chip of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

With initial reference to Figure 1A, a programmable analog system is provided on a single integrated circuit chip having one or more signal inputs 801, one or more signal outputs 803 and configuration data input 805 pins, among others. Analog signal input modules 807-809 and analog signal output modules 811-813 allow for connection of the input and output pins, respectively, to a configurable interconnection network 815. The input modules 807-809 can also include programmable circuit functions, such as buffering, filtering, switching, and other signal conversion functions that enable the chip to be adapted for use in a wide variety of types of analog systems. Similarly, the output modules 811-813 can provide programmable buffers, switching circuits, comparators, and the like. If the circuit chip is designed to interface directly with a digital system, an input module can include a digital-to-analog converter,

and an output module can include an analog-to-digital converter. For many applications, there is no need for any other digital processing of the signals being processed by the chip, all the signals otherwise being in analog form. However, such digital signal processing can be included where useful.

A plurality of functional analog circuit modules 817-819 are connected to each other, and to the input modules 807-809 and output modules 811-813 through the configurable interconnection network 815. A wide variety of analog circuit functions can be included in individual ones of the functional modules 817-819, such as amplifiers, comparators, adder/subtractors, filters, rectifiers, and other normally used analog circuits. An individual functional module preferably includes a more complex circuit that is programmable by the user to perform a selected one of two or more such functions. Operating parameters for each selectable function are also programmable, such as the gain of an amplifier, the bandpass characteristics of a filter, the threshold characteristics of a comparator, the level of hysteresis of a comparator, and similar known analog circuit parameters.

It is also desirable to provide one or more support modules 821 not directly connectable in the analog signal path but which provide support to other modules or configuration circuitry. One example is a bias voltage or current generator whose voltage, current or other characteristic of its output is programmable. Another is a clock oscillator having programmable frequency clock signals. A programmable auxiliary circuit 823 is also desirable. A test module 825 allows connection of a pin 827 to a selected node within the interconnection network

815. Programmable power control circuits 829 are also desirable in order to specify which modules are to operate in a reduced power state during periods of non-use.

In order to program all the modules in the system and interconnect the input, functional and output modules together to form a customized operable analog circuit between the input and output pins, a digital configuration circuit 831 is provided. Data loaded through pin(s) 805, in serial or parallel form, is used to make connections within each of the other blocks shown in Figure 1A. In a preferred form described in more detail with respect to Figures 1C-10, the configuration circuit 831 includes a plurality of series connected registers which are loaded with configuration data through the configuration data input pin(s) 805. Those registers are of a volatile type but could be formed on non-volatile memory if desired. Specific fields of the configuration data registers are connected to program operation of individual modules and to interconnect them through the network 815. A capability is also provided to dynamically change the contents of individual ones of the registers during operation of the circuit, thus allowing a host system in which the circuit chip is used to reconfigure at least one function, connection or operating parameter of one or more modules, an ability that is not available with usual analog circuits. Configuration data to be loaded into these registers upon initialization of the circuit chip may be stored in non-volatile memory provided on the chip in a manner that any dynamic changes made during operation do not affect the contents of the memory.

The interconnection network 815 may be implemented in a number of ways. It can be a full cross-bar type of network, for example, in order to allow a

maximum flexibility of the interconnections which are possible. However, since only a limited number of connections need be provided, as will become more apparent from later descriptions herein, the overhead associated with such a network is not justified. Therefore, a more limited type of interconnection network 815 is utilized. This may be one of the many types used in or proposed for field programmable gate arrays (FPGAs) but those networks are also usually more complex than necessary. The specific devices used within the network 815 to make selected interconnections between conductors can also be selected from a wide variety of known types, such as fuses, anti-fuses or volatile pass transistor switching networks. The later type of switching device is preferred herein since this allows easy reconfiguration, including the making of changes in the circuit as part of its operation.

A preferred interconnection network 815 is illustrated in the somewhat more specific system of Figure 1B. The module interconnection network 815 includes a bus having a number of signal paths (signal highway) with one or both of the internal input or output of the individual modules being connectable to one or more of the internal bus signal paths. In this example, the bus is shown in two portions 833 and 835, joined by a switching network 837. The switching network 837 can be designed to connect various ones of the conductors of the bus portion 833 to those of the bus portion 835, or simply be able to break certain of the bus conductors into two isolated segments. Any such connections can be placed under the control of the configuration circuits 831, and are useful when a larger number of modules is utilized. It is not employed

in the specific embodiment described with respect to Figures 3-7, wherein a single bus segment exists.

The connection of the modules to specific conductors of the bus segments 833 and 835 is shown in Figure 1B with a high degree of generality. The input modules 807-809 have their individual outputs connected to a selected one or more of the bus conductors through switching circuits 839-841, in response to respective control signals from the configuration circuits 831. Similarly, the output modules 811-813 have their individual inputs so connected through switching circuits 843-845. The functional modules 817-819 have inputs connected to one or more bus signal paths by switching circuits 847-849, and outputs by switching circuits 851-853. A switching circuit 855 connects one or more of the conductors of the bus to the test module 825, for outputting through pin(s) 827.

Such a high degree of flexibility in controlled connections of the modules to the bus is usually not necessary, however. However, either all the module inputs or outputs may be permanently connected to a unique bus conductor. The other of the internal input or output of the individual modules is then selectively connected to a designated number or all of the bus signal paths by switching circuits, in response to control signals from the configuration circuits 831. This more limited interconnectability is implemented in the embodiment of Figures 1C-10 described below.

The functional modules 817-819, and to some extent the input modules 807-809 and output modules 811-813, may be made to operate with either voltage or current analog signals. The best type of circuit technique to be employed within the modules depends upon the frequency

range, bandwidth, voltage swing, noise tolerance and other characteristics of signals with which the circuit chip is expected to be used. In either case, the internal input and output interfaces of the interconnectable modules are constructed so that their operation and effect on the analog signals are substantially independent of which other modules are interconnected together and any variations of impedance or other characteristics between specific module interconnections. The modules are constructed to be interconnected together in a wide variety of different combinations according to the desired overall circuit intended to be configured, all without the quality of the analog signal or operation of the individual modules being adversely affected by any of a large number of different possible connection paths being utilized between the input, functional and output modules.

In the case where the signals are carried within the individual modules by a varying voltage (voltage mode) and communicate voltage varying signals between modules, the input impedance of each such module is made to be very high, and the output impedance is made to be very low. In the case where the modules carry signals as current variations (current mode) and communicate current varying signals between modules, the input impedance of each such module is made to be very low and its output impedance made to be very high.

A more specific implementation of the architectural features of the present invention is illustrated in Figure 1C, which is provided on a single integrated circuit chip. Several pins of the circuit chip are designated for receiving input signals, a single line 11 and a group of lines 13 being shown connected to such pins. Similarly, several of the circuit pins are

designated for carrying output signals, lines 15, 17 and 19 being individually connected to such pins. The input signals are applied to a circuit configured from a plurality of functional analog circuit modules, three such modules 21, 23 and 25 being illustrated in this example. Generally, many more such modules are included on a single integrated circuit chip.

Each functional module contains an operating circuit. The analog circuits implemented by individual functional modules include one or more amplifiers, one or more comparators, filters, and the like, at least some characteristics of which are programmable by the user. This is preferable to providing a mere assembly of transistors which must be programmably interconnected in order to form any operable circuit. As described in more detail later, the characteristics of the circuits which are programmable by the user include the gain of an amplifier, the threshold characteristics of a comparator, the bandpass characteristics of a filter, and the like. An individual functional module usually includes one such circuit but can alternatively have two or more such circuits. Also, one or more modules may be included that contain only passive components, such as a programmable resistor or capacitor circuit. The particular functions that are provided in the plurality of functional analog circuit modules included on any particular integrated circuit chip will, of course, be selected to be those useful for the range of applications for which the circuit chip is being provided.

In addition to the plurality of functional modules processing the signals between the input and output pins if the circuit chip, circuit modules are also included at the input and output of the circuit. For

example, an input circuit module 27 receives a signal in the line 11 and outputs it in a line 13. The input module 27 is shown not to be configurable; that is, its characteristics are fixed. If designed to receive an analog signal in the line 11, the module 27 can include a bandpass filter, or a buffer amplifier, circuits to bias the input signal, and the like, either individually or in some combination. All of these functions can be made to be programmable in the same manner as the other input module 33 but is non-programmable in this specific example. Lines 29 and 31 extend from the input module 27 to respective external pins of the circuit, something that is useful for connecting an external capacitor to a filter circuit within the module 27, for example. This external connection can be turned on and off by an additional programmable configuration bit, if desired. If the input signal in the line 11 is in digital form, the input module 27 contains a digital-to-analog converter (DAC) and usual types of analog circuits as are provided at the output of a DAC.

A different type of input module 33 is also illustrated in order to show other possibilities. One of several input lines 13 is effectively connected to an output line 35. The input module 33 can contain any or all of the circuit functions described with respect to the input module 27. A major difference, in this example, is that module 33 has some characteristics which are configurable by the user, one such characteristic being the selection of one of the input lines 13.

Similarly, output modules are provided, two such output modules 37 and 39 being shown in the example system of Figure 1C. Typically included in an output module is a buffer amplifier but other circuit functions may also be

included, such as a filter, comparator and the like. The output modules will also contain an analog-to-digital converter (A/D) in cases where a digital output is desired. Other than the possible inclusion of input DACs and output A/Ds, no other digital circuit elements are included in the signal path between the signal input and output pins. However, digital circuitry is included to control the internal configuration of the various modules and their interconnections.

Each of the input, functional and output signal modules described above are interconnected over a bus 41 (signal highway). Each signal path of this example bus 41 is a single electrical conductor, or pair of conductors, depending upon the type of analog signal that is being communicated over the bus. In the example architecture of Figure 1C, the outputs 13 and 35 of the input modules, and outputs 22, 24 and 26 of functional modules, are permanently connected with a unique one of the signal paths of the bus 41. The inputs to the functional and output modules are selectively connected to individual signal paths of the bus 41. That is, the specific bus signal paths to which the module inputs are connected are programmable by the user. This arrangement is advantageous when the modules operate in a voltage mode, since the module outputs can simultaneously drive more than one other module. However, this is preferably reversed for a chip where the modules operate in a current mode, namely the inputs of the functional and output modules are permanently connected with unique ones of the bus signal paths, and the outputs of the input and functional modules are selectively connected to various of the signal paths. This is because the inputs of current

mode modules can accept more than one current output of other modules.

As a further alternative scheme for connecting the modules to the bus 41, all of the module inputs and outputs can be programmably connected to the bus signal paths. This provides the most flexibility but the resulting level of complexity, in additional switching circuits and associated control circuitry, is usually unjustified. Further, the interconnection arrangement of the embodiment of Figure 1C has a significant advantage in that only one switch is required to interconnect two modules together. That is, since one of the input or output of the individual modules is permanently connected to a unique circuit of the bus 41, two modules are connected together by operation of only one switch in the other of the input or output of one of the modules. This gives a predictable series impedance between modules, no matter what arrangement is chosen for their interconnection. Problems associated with interfacing modules together increase if the number of switches, and thus the level of series impedance between modules, varies significantly.

All of the signal modules described above, except for the input module 27 in this example, are configurable either as to the characteristics of the analog signal circuits included in them, or the signal paths of the bus 41 to which they are connected, or both. The configuration circuits within each module are indicated by a dashed rectangle, such as circuits 43 within the input module 33, circuits 45 within the functional module 25, circuits 47 within the functional module 23, circuits 49 within the functional module 21, circuits 51 within the output module 37 and configuration

circuits 53 within the output module 39. Each of these internal module configuration circuits includes a shift register. These shift registers are connected in series to receive configuration data over circuits 55. That is, binary data is serially shifted along this series connected number of shift registers to reach desired configuration circuits within one or more of the modules. The serial input circuit 55 through which such a binary signal is introduced includes one line for the binary signal, a clock line for providing clock signals to each of the shift registers in order to move the data through them in sequence, and potentially other control lines required to bring this about. These lines are extended between the output of one shift register to an input of another shift register, such as by a segment of lines 57 extending between the configuration circuits 43 and 45, a segment 59 between the configuration circuits 45 and 47, and so forth. In addition, each of these configuration circuits receives additional control signals over lines 61. Signals in the lines 55 and 61 are generated by a configuration control circuit 63.

A user of the integrated circuit chip of Figure 1C serially loads this binary configuration data through a pin of the circuit's package onto a line 65, along with an accompanying input clock signal in another line 67 from a separate pin. A load control signal applied to yet another pin provides a signal in the line 69 which operates to both select the chip for receiving configuration data and to latch that data into each of the modules' configuration circuits after receipt. A load control output signal in a line 71 is generated for use when several chips are connected together in a daisy chain

arrangement, as discussed below with respect to Figure 11A.

A non-volatile memory 73 is provided as part of the integrated circuit chip in order to store the configuration data desired by the user to be initialized in all of the modules' configuration circuits. The preferred type of memory is an EEPROM, although some other type of read-only-memory (ROM) may be employed instead, particularly if it is not required to reprogram the memory 73. Such other ROMs include flash EEPROM, EPROM, fuse, anti-fuse, and the like.

Configuration data is loaded by the user into the memory 73, when an EEPROM or other such programmable type, through the line 65 along with the user's clock signal in line 67, and then by way of circuits 74. Since the configuration circuits within each of the modules includes volatile memory, the configuration data is written into the modules from the memory 73 upon the circuit chip being powered up. This internal operation is synchronized to an internally generated clock signal in a line 76 from a clock oscillator 75. The configuration data stored in the memory 73 is shifted with the internal clock signal in line 76 into the series circuit of configuration shift registers through circuits 55. Because of the rewriting capability of an EEPROM, the memory 73 may be reloaded periodically by the user, as desired. Any capacity of the memory 73 in excess of that required for the configuration data can be used for general storage purposes within a system in which the circuit chip of Figure 1C is employed. General storage data is read in and out of the memory 73 through the same serial path as used to load configuration data.

The configuration data stored in the memory 73 can remain in the configuration circuits of the modules without change during operation of the circuit but the configuration capabilities of this circuit also allows the user the periodically change the configuration of all the modules or a selected one or more of them at a time, during operation of the system. This new configuration data is applied through the input lines 65, 67 and 69 from their respective pins.

Referring to Figure 2, the circuits which allow the user to reconfigure a selected one or more modules during operation of the system of Figure 1C is described. A semiconductor switching circuit 77 allows a control circuit 79 to direct configuration data inputted through the line 65 to either a shift register 81, another switch 83, or an input of the non-volatile memory 73. The switch 83, also operated from the control circuit 79, connects the input serial configuration data lines 55 to either receive such data from the on-board memory 73 or from the external configuration data input 65. The switch 83 also simultaneously selects the internal clock signal on line 76, when data is being loaded from the memory 73, or the external clock in the line 67, when the user is loading configuration data directly into one or more modules.

Such externally loaded configuration data has a format illustrated in Figure 3A. When the load signal in line 69 goes from an inactive to an active state, the control circuit 79 is set to accept configuration data in the line 65. A first byte 85 of such data is received by the shift register 81 of the circuit of Figure 2, with the switch 77 appropriately set. Those bits are applied in parallel over lines 87 to both a decoding circuit 89 and a digital counter 91. This first byte 85 is operated upon

by the decoding circuit 89, in response to control signals over lines 92, in order to generate an active signal in one or more of output lines 93. The command byte 85 can be used to set a number of internal operations within the integrated circuit chip but only the operation of loading configuration data into one or more modules is explained here. The command byte 85, when designating such a configuration operation, also provides the address of the module into which configuration data to follow is to be loaded.

The configuration circuits 43 and 45 of two of the modules 33 and 25 are included in Figure 2 in order to illustrate operation of the circuit. Each configuration circuit includes a separate enable line as part of the configuration control circuit 61, an enable line 95 being connected to the configuration circuits 43 and an enable line 97 being connected to the configuration circuits 45. The command byte 85 is decoded by the circuits 89 to enable one of the configuration circuits 43, 45, etc. for receiving the configuration data that follows.

As an example of the structure of each of the configuration circuits within the individual modules of the system of Figure 1C is shown in Figure 2. Typically, the configuration circuit 43 includes a shift register 98 that is either included within the series connection of shift registers or bypassed, depending upon the setting of semiconductor switches 99 and 100. These switches are set by the select signal in the line 95. If the configuration circuits 43 are addressed by the command byte 85 (Figure 3A) of the data being received in the line 65, then the switches 99 and 100 are actuated to connect the shift register 98 in the series circuit. Otherwise, the switches 99 and 100 cause the configuration data being

loaded to bypass the shift register by substituting a conductive path 101. Although semiconductor switches are schematically shown in Figure 2 as a convenience in explaining the operation of the circuit, logic gates, such as two or more NAND gates, connected in the form of a multiplexer (MPX) are usually employed to perform the switching function.

The term "shift register" as used in the foregoing portion of this description is meant to refer to a group of storage cells, in the long series connected circuit formed of such cells, which can be bypassed by a single switching circuit of the type just described. Additionally, the term "shift register" is also used later in this description (see Figures 40 and 41, for example) to refer to a portion of a module's shift register which carries a certain field of configuration data, or to a portion which carries one of a plurality of sets of different configuration data that is selectable by a switching signal to be connected with the module. Further, the term "shift register" is also used later in this description to refer to a plurality of shift register cells that are physically grouped together as a unit, separated by conductors from other such groups. The number of bit cells included in a "shift register" referenced herein is made clear from the context in which it is used.

In the case of the configuration circuits 43 being addressed, for example, the shift register 81 receives the next byte 103 of the configuration data (Figure 3A) which is then used to set the digital counter 91. The byte 103 gives the number of bits of data 104 (Figure 3A) which follows. The digital counter 91 having been loaded with that number, the switch 77 is activated

to send these data bits 104 into the configuration data circuits 55. As each bit occurs, the digital counter 91 is decremented by 1. When the counter 91 reaches "0", the circuit 63 then knows that all of the data bits to be received have indeed been received and that any further bits are from a command byte of another configuration data transmission. In the example where the configuration circuits 43 have been selected, the number of data bits loaded are determined by the capacity of the shift register 98. The serially connected shift registers in each of the modules can have different capacity depending upon the number of choices provided for operation of the modules controlled by the data stored in the register.

The control circuit 79 generates a load command signal in a line 70 in response to the load input command signal in the line 69 returning to an inactive state after configuration data has been loaded. Data loaded in the shift register 91 are then latched into a configuration register 105, in response. This data are then decoded by a decoding circuit 106 to give in line 107 control signals to various transistor switches to configure operation of the input module 33. The configuration circuits 45 of the functional module 25 operate in the same way, except, in this example, its decoder outputs control signals in lines 108 to designate the signal paths of the bus 41 to which its inputs are connected and, through control signals in lines 109, the internal configuration and operation of the functional module.

The various shift registers and configuration registers are, in most applications, formed of volatile static random-access-memory (SRAM) cells. However, they may, in the alternative, be formed of other types of cells within the rather extensive memory technology. Further,

the shift registers may be of one type and the configuration registers of another type. Non-volatile floating gate EEPROM technology is quite suitable for the configuration registers. If reprogrammability is not contemplated, the configuration registers may be formed of fuse or anti-fuse elements, being programmed one time from configuration data loaded in the shift registers. Mask programmed read-only-memory (ROM) may also be used for the configuration registers when only one configuration of a large number of circuit chips is desired, thus eliminating the need for the serial connection of shift registers and reprogrammability generally. A one time programmable or pre-programmed circuit chip does not have, of course, the same flexibility of configuration and reconfiguration being discussed herein but reduces overhead of the circuit by eliminating the shift registers, non-volatile memory and the test probe module. Alternatively, not all of the configuration registers are permanently programmed, leaving one or a few of the configuration registers to be reprogrammable by providing accompanying shift registers.

Referring again to Figure 1C, other similarly configurable modules may be used which are not in the signal path between input lines 11 and 13, and output lines 15, 17 and 19. Such additional modules include configuration circuits connected in the same series circuit as the configuration circuits within modules which operate upon the signal. One such module is a test probe module 110 which includes configuration circuits 111 for connecting an output 112 to any one of the signal paths of the bus 41. This allows for the user of the integrated circuit chip to have direct access for test purposes to signals on the bus 41 internal of the chip. The test probe module may also include one or more amplifiers,

optional filters, and the like, in a signal path from a selected bus circuit to the output 112, any of which can be made to be programmable from the configuration circuit 111. Another module 113 includes configuration circuits 114 that set bias levels in one or more lines 115 that are utilized by other analog modules of the system.

It is also sometimes desirable and useful to provide a reference voltage output in a line 116, so a module 117 may be provided for this. The reference voltage is set by loading desired configuration data into circuits 118. Similarly, it is sometimes desirable to include an analog signal module 119 that has both inputs 120 and an output 121 connected to external pins. A configuration circuit 123 configures the operating parameters of the circuit 119. This circuit can be, for example, an amplifier whose gain is set by the configuration bits loaded into the circuits 123, or some other or more complicated analog circuit.

The clock oscillator 75 is optionally made to be configurable by including configuration circuits 72 in the configuration data chain. Such configuration can include the setting of frequency dividers in order to set the output frequency or frequencies of the clock circuits 75.

Referring to Figure 3B, an example of the contents of the module configuration registers of Figures 1C and 2 is given. These contents are illustrated in the form of a bit stream that is one bit wide, representing that which is loaded into the registers of Figures 1C and 2 from the control circuits 63 during initialization of the circuit chip described with respect of Figures 1C-10. In the example of Figure 3B, one group 869 of contiguous bits is positioned in the bit stream so that it is loaded into the configuration register 43 (Figures 1C and 2) of

the input module 33 (Figure 1C). A next contiguous group of bits 871 is loaded into the configuration register 45 of the functional module 25. A group 873 of bits, appearing later in the bit stream, becomes loaded into the configuration register 48 of the input module 27, a group 875 in a configuration register 51 of the output module 37, a group 877 into the configuration register 123 of the auxiliary module 119, and a group 879 loaded into the configuration register 72 within the clock oscillator module 75. Similar groups of bits exist for each of the other configuration registers shown in Figure 1C but are omitted from Figure 3B for simplicity.

Each such group of bits includes several fields. For example, the group 869 (Figure 3B) which controls the input module 33 (Figure 1C) includes a field 881, the bit values of which control the gain of an amplifier therein. The bits in another field 883 control the power of the input module, designating whether that module is powered down individually when it is not used and/or whether it is powered down upon a global power down command. Another field 885, in this example being only one bit, designates whether the filter 125 of the input module 33 is to be included in the circuit. Another field 887 controls operation of the multiplexer 124 of the input module 33. The binary contents of this field can either directly control the switching operation of the multiplexer 124, or control whether or not the multiplexer 124 is switched in response to signals from external pins over lines 861, or both. This particular module example, as with the others being described is meant to be exemplary of the types of things that can be controlled by the configuration bits within the one bit stream that are designated for loading into a particular module.

The group of bits 871 (Figure 3B) includes a field 889 which controls the gain of the amplifier within the functional module 25 (Figure 1C). A field 891 controls the power saving operation of this module, as is the case with most of the other modules. Another field 893 controls whether one or two inputs are to be used, and their respective polarity. A final field 895 designates which of the conductors within the bus 41 the inputs of the module 25 are to be connected.

A field 897 in the group of bits 873 sets the gain of the amplifier within the input module 27, and another field 899 controls its power down response. Another field 901 designates whether the filter of the input module 27 is to be used or not, and, if so, whether the external connections 29 and 31 are to be provided. These external connections can be used to add a capacitor or other off chip component to the on chip filter of the input module.

For the output module 37 (Figure 1C), a field 903 (Figure 3B) sets the output voltage of a voltage reference circuit. This circuit can be configured to be, in effect, an analog-to-digital converter. Another field 905 of bits sets the operating mode of the output module. These bits select whether the module operates as a simple buffer amplifier, which then does not utilize the voltage reference source 863, or as a comparator, when that reference source is used. Another field 907 controls the power down response of the module 37, and another field 909 establishes a connection between the input circuit 867 and one of the signal paths within the bus 41.

By decoding the contents of a configuration register field, a number of switches may be controlled which greatly exceeds the number of bits in the field

being decoded. This is usually preferable to dedicating each individual configuration register bit location to control the state of a single switch. The sizes of the shift and configuration registers are thus minimized.

The ability to individually address and rapidly load data into a single, or a few, of a large number of configuration registers in one operation is a significant feature of the chip architecture described above. Even though the shift registers are connected in the usual series circuit, they are randomly addressable for the loading of configuration data in them. This allows dynamic configuration of the operation and/or changes in connection of one or more selected modules while the system is processing actual analog signals. Yet no more than the usual small number of pins of a serial data transfer system is required. Shift register stages associated with a particular module are preferably positioned on the integrated circuit chip near that module, in order to reduce the length of switch control lines that extend from the register decoders to switches in or associated with the module. The distributed shift register stages are then connected together by just a few conductive paths for the serial transfer of data along and control of the string of shift registers.

In a preferred embodiment, the dynamic configuration does not affect the contents of the non-volatile memory 73. That is, the configuration registers are loaded with the unchanged contents of the memory 73 the next time the chip is powered up, regardless of any changes which were previously made directly to the contents of the configuration registers. This system also has applicability to the configuration and interconnection

of digital modules in a field programmable gate array (FPGA).

An example structure of an input module 33 is illustrated in Figure 4. An input selection switch 124 connects one of the input signal lines 13 to a filter circuit 125 in accordance with the state of the signals in control lines from a switching and logic network 88. Many different arrangements may be implemented but that in Figure 4 provides the network 88 to respond to control signals in lines 107 from the configuration circuits 43 to either select one of the input lines 13 by setting the switch 124 directly, or, to connect lines 84 from external pins to control the setting of the switch 124. With the later selection, external signals through lines 84 control the switch 124. This more easily enables dynamic switching of the multiplexer 124 in order to time share the resources of the circuit chip among several input signals. The selected signal, after passing through a filter 125, is then amplified by an amplifier 126. The example of Figure 4 allows for the filter 125 to be programmed in response to additional configuration bits, and the amplifier 126 to have its gain or other operating characteristics similarly controlled. Many variations are possible to accommodate specific applications for which the circuit chip is designated. The filter 125 can be connected to two circuit pins for the connection of an external capacitor, if desired by the user, such as described earlier with respect to the input module 27. The implementation of this external circuit connection can also be turned on and off by further configuration bits. Also, an offset or bias of the input signal may be introduced at the input to the amplifier 126, the amount

being set by other configuration bits. The flexibility of the implementations being described is quite wide.

Similarly, an example structure of the functional module 25 is shown in Figure 5. The heart of this module is a circuit cell 127 whose characteristics are configured by signals in the lines 109. Examples of such circuit cells are described in detail hereinafter. This circuit cell 127 is shown to have two inputs 128 and 129, each of which is independently connectable to a selected signal path within the bus 41. Each of the circles of Figure 5 represents a semiconductor switch that is activated to either connect or disconnect one of the input lines 128 and 129 to one of the bus signal paths in response to a control signal in one of the lines 108. In an implementation where each bus circuit is formed of two or more lines, two or more switching circuits are thus utilized in place of the one shown, one for each line. It will be noted from Figure 5 that no switching circuits are provided to connect either of the input lines 128 and 129 to the signal path within the bus 41 to which the output 26 is connected. Such connections may be made possible, however, and then restricted by other controlling circuits or programming software. Circuit cells of other functional modules can alternatively have only a single input and/or two outputs, depending upon the specific function being provided.

The circuit of Figure 6 shows, as an example, the output module 39 to include two comparators 134 and 135, each of which has one respective input 136 and 137 that are individually connectable to a signal path of the bus 41 in response to appropriate signals in lines 138 from the configuration circuits 53. The second input of each of the comparators 134 and 135 is a reference voltage

from respective sources 139 and 140 which are set to a level designated by signals in respective lines 141 and 142 that result from other configuration bits loaded into the configuration circuits 53. The reference voltage sources are digital-to-analog converting circuits. This output circuit provides a window comparator. This is effectively an A/D converter, providing a digital output in lines 17 and 19. Each of the two output paths of the module 39 can, however, also be independently programmed, in response to configuration bits in its configuration circuit 53, as a simple window comparator or as a buffer amplifier. A single comparator and voltage reference source can also be utilized in the other output module 37 to provide a selection of operation as a comparator, thus providing a simple digital output, or as a buffer amplifier, thereby providing an analog output.

Figure 7 illustrates the test probe module 110 of Figure 1C. It includes a buffer amplifier 130 having an input line 131 that is connectable to any of all or nearly all of the signal paths within the bus 41. One of the cross-point switching circuits shown may be activated at a time to connect the input line 131 to a selected one of the signal paths of the bus 41, in response to an appropriate switching signal in one of the lines 133 from the configuration circuits 111. The configuration circuit 111 includes the same structure as the circuit 43 described with respect to Figure 2.

Each of the circles in Figures 5-7 represents a cross-point switch, an example of which is illustrated in Figure 8. One of the cross-point switches of Figure 7 is specifically illustrated. In a CMOS implementation of the circuits being described, two complementary transistors M1 and M2 are connected in parallel between two lines 41' and

131 which are desired to be selectively connected together. A switching control line 133' is connected to the gate of one of the transistors, and through an inverter 143, to a gate of the other transistor. When a voltage on the line 133' is at one level, the transistors M1 and M2 are turned off, and when this voltage is of another level these transistors are turned on. When on, the module line 131 is electrically connected to the bus line 41'. When off, no such connection is made. Of course, other specific switching circuits may be alternatively used. The structure of the analog cells of the modules which are interconnected, as described below, greatly relaxes the precision with which such switching transistors must be formed. That is, their "on" resistances may vary significantly from chip to chip, and under varying operating conditions of a single chip, without affecting operation of the respective analog cells that are connected together through those switches.

Figure 9 illustrates the internal bias generator 113 of Figure 1C. A bias generating circuit 144 receives a voltage or current supply, as appropriate, in a circuit 145. An output level of that current or voltage in a line 115 is controlled by signals in lines 146 which are set by the configuration data that is loaded into the configuration circuits 114 of the module 113. An application of such a bias generator is to provide the offset voltage mentioned above for the input module 33.

Similarly, with reference to Figure 10, the auxiliary module 119 can contain an analog circuit 147, such as an amplifier, comparator or the like, having an operating characteristic such as amplifier gain or comparator level controlled by signals in lines 148 that

are set from the configuration bits loaded into the configuration circuits 123 of that module.

The particular structure and use of the bus 41 that has been described to interconnect the input, functional and output modules is preferred when the number of such modules is not large, less than about 20. In addition to allowing all possible connections, each connection between modules is made with only one cross-point transistor switching circuit in the signal path. This minimizes one source of variations in the impedance of connections between modules that exists if connections are made with a variable number of such switching circuits. The impedance of connections between different modules can still vary because of different signal path lengths which these interconnections can take and some variation inherent in the impedance characteristics of the transistors on a single chip which form the cross-point switches.

At some higher number of modules, however, depending upon the specific implementation, the amount of semiconductor chip area consumed by having so many signal paths as part of the bus structure can become more than desired. In such cases, a more general cross-bar or partial cross-bar switching circuit may be preferred, even though the number of transistor switching circuits connected in series to form specific interconnections between modules on a single configured chip can vary from one to several. Added flexibility can alternatively be included in the system described above by segmenting the bus with the addition of switching circuits in the path of the individual bus lines for the purpose of controllably interchanging the bus lines or isolating their different segments from each other. Any of these more complicated

switching circuits will be controlled by one or more configuration registers separate from those of the modules themselves but connected in the same series circuit of registers that is used to load data into those in the modules.

In any event, the input, functional and output modules are designed be insensitive to the variations in impedance that can exist in the signal paths between them when the chip is configured. The analog circuits within the modules are also designed to be insensitive to interconnection variations caused by changing operating characteristics such as temperature. These characteristics are further discussed in another section below in connection with a description of examples of such modules.

Use of More than One Such Chip

Referring first to Figure 11A, however, the use together of two or more chips 1, 2, 3, etc., each of the type described above, will be explained. Multiple chips provide a multiple of the functional modules of one chip for use as a single system. The architecture of the individual chips allows several of them to be configured as a single unit. Although the configuration data in line 65 and the clock signal in line 67 are applied to each of the chips, the load control signal in line 69 is not connected to each of the chips. Rather, it is connected to only the first chip 1, while the output load control signal 71 of the chip 1 is applied as an input load control signal 69' to the second chip 2, and so on, in a daisy chain arrangement.

The control unit 79 (Figure 2) of each of the chips 1, 2, 3, etc., operates in the following manner:

When the load input signal 69 first goes active in preparation to receiving configuration data, the control unit 79 of the first chip 1 resets its counter 91 and renders the load output signal 71 inactive. The control unit 79 of the second chip 2 thus renders its load output 71' inactive, and a similar result is obtained for all other chips along the chain. The configuration data (of the form of Figure 3A) applied to all of the chips over the line 65 is, as a result, accepted only by the first chip 1. The command byte 85 is decoded by circuits 89, the counter 91 set to the number of data bits 103, and the data bits 104 are then received until the counter 91 reaches a zero count. The control unit 79 of the first chip 1 then causes its load output signal in line 71 to become active. The next configuration information of the form of Figure 3A is then accepted by the second chip 2 in the same manner as just described for the chip 1. The control unit 79 of the chip 1 does not allow that chip to recognize this second unit of configuration data, even though its load input signal remains active, since nothing has occurred to reset its counter 91. The chips downstream of chip 2 remain inactive because their load control signal inputs (input 69" of chip 3, for example) remain inactive. After configuration data is loaded in the chip 2, the process moves to a third chip in the chain, if one exists, and so forth.

After all the configuration data is loaded into shift registers of all the chips 1, 2, 3, etc., of the chain of chips, the load signal applied in the line 69 to the first chip 1 is caused to become inactive. This causes, through operation of the control unit 79 in each of the chained chips, the load output control signals 71, 71', etc., to also become inactive. The control unit 79

of each chip also responds to each of their respective load input signals going inactive, after the loading of their configuration data, to emit a load signal in the line 70. This causes the data loaded into the shift registers of each of the chips to be latched into their respective configuration registers.

Applications

There are many actual and potential applications of the circuit chip being described. A primary application is the rapid prototyping of an analog circuit. After the chip(s) is programmed and configured to provide an operating circuit that, as determined by actual tests, has the desired characteristics, the resulting circuit may be replicated by loading the same configuration data into other such chips. A small volume of such customized integrated analog circuits may be economically produced for incorporation into electronic systems. This saves the very significant expenses associated with designing and producing custom integrated circuits. For large volumes, however, the configuration data can be used to design and produce a custom integrated analog circuit, when the large investment in doing so is made worthwhile by the volume involved. Another advantage of using the configurable chip of the present invention in production systems, rather than using a dedicated circuit custom chip, is that it can be made much more difficult for a competitor to determine by reverse engineering the analog circuit implemented by the chip. Since the programming and configuration data is stored in memory, opening of the chip will typically destroy the contents of the memory.

The ability to dynamically program and configure the analog circuit chip of the present invention opens a

range of other applications. In response to varying conditions, the chip can be reprogrammed while in operation, in the manner described above, to adjust to the new conditions. One example of such a changing condition is a change in the amplitude of a signal connected to the chip. Examples of longer term changes for which compensation may be provided are those brought about by circuit drift, aging, and the like.

The circuit chip of the present invention may also be used as part of an analog or digital system in order to introduce some level of programmability to that system. The dynamic reprogramming capability of the chip of the present invention can be used for this purpose. Examples of such programmable system functions include multi-purpose printed circuit boards for generating signals, receiving signals, or converting signals. One or more chips according to the present invention can be used as part of such boards to allow changing characteristics of signals being generated, changing characteristics of the signal processing of signals being received, and the like.

Another attractive application of the circuit chip of the present invention, is to access a variety of analog signals in a system. Such a chip can be used to monitor or test another analog system by either sending signals to that system or accessing signals within that system. Accessed signals can then be adaptively conditioned or converted before forwarding to test equipment. Such a use is generally illustrated in Figure 11B. The electronic system being monitored is generically represented by three interconnected blocks 4, 5 and 6, which can individually be circuit chips and/or printed circuit boards, analog and/or digital. One or more chips

7 of the present invention has its inputs 8 connected to various nodes of the system being monitored. Signal outputs of the one or more chips 7 are provided in lines 9. The configurable analog chip of the present invention may thus be used as a test probe for internal nodes of an operating system. It may look at individual signals at those nodes, the difference between two signals, and/or perform other similar functions.

The application illustrated in Figure 11B also allows the configurable circuits of the present invention to be used in a watchdog mode. Periodically, the chip(s) 7 monitors various signals to see if they are within preset limits. A signal is then outputted when some signal falls outside this range.

Voltage Mode Operation

With reference to Figure 12, certain aspects of continuous voltage mode operation are illustrated. A first module cell 151 is illustrated with its output connected to an input of a second voltage mode cell 153 through interconnection circuits 155. The interconnection circuits 155 include the bus 41 (Figure 1C) and at least one, and perhaps several, switching circuits of the type illustrated in Figure 8. Although the interconnection bus system of the embodiment of Figure 1C has the advantage of requiring only one such switching circuit to interconnect two modules, as previously discussed, the individual modules can have a varying number of switches within the modules at their inputs or outputs. Also, the interconnection circuits 155 may in some cases include a short conductive path and in other cases be a very long conductive path. The impedance characteristics of the interconnection circuits 155 can also vary among different

circuit chips, as a result of process variations, and those of a given chip will vary as a function of its operating temperature. And if a different type of interconnection network is used where the number of switches in the signal paths between modules can vary, such as in a more general cross-point switching network, the impedance of connections between modules can vary considerably. Therefore, when any one of these or other causes of variations in module interconnection impedance can exist, it is highly desirable to design the analog circuit cells in accordance with criteria that make their operation and signal communication independent of the value of potentially wide ranging interconnection impedance.

One constraint which is imposed is that the input of each analog cell is of a very high impedance with respect to the maximum expected interconnection impedance by a factor of at least 10 and preferably 100 times. An infinite input impedance is preferable. If any substantial amount of current is drawn by an input to an analog voltage mode cell, a buffer amplifier or some other device is inserted which draws substantially no input current, thereby eliminating the effect of a varying interconnection impedance upon the actual value of current that is drawn by that input to the cell. None of the functional or output modules of the system of Figure 1C are permitted to draw any substantial amount of input current.

The goal of a high input impedance (resulting in a low input current) is to minimize any voltage drop across the interconnection circuits (primarily the "on" resistance of the switching transistors which are rendered conductive) in the path of the input signal. Such a

voltage drop creates an error in the signal. It is desired to keep the effect of this error at a level less than about 0.1%, and preferably less than about 0.01%, of the effect of other error sources. Such other error sources include amplifier gain errors, offset errors, and the like.

Similarly, the output of the voltage mode cell is constrained to have a very low impedance with respect to the lowest possible impedance of an interconnection circuit with the input of another cell, at least by a factor of 10 and preferably 100 or more. The outputs of individual input and functional modules of the system of Figure 1C have the capability to drive the inputs of one, two, or more other modules to which it may be connected through the bus 41 and switching circuits.

Figure 13a shows a simple inverting amplifier having a signal input 155 and a reference 157. The reference 157 is often ground potential, but for reasons explained below, the reference in some specific circuits may be a voltage other than ground potential so this is being generalized in this description. A differential amplifier 159 has a tapped resistor R1 that provides a feedback resistance and an input resistance, the ratio of which determines cell gain. Since a current is drawn through the input line 155 by such a circuit, a buffer amplifier 161 of unity gain is interposed between an input of the analog cell and the inverting input of the amplifier 159. This then satisfies the criteria set forth above for the high input impedance. The output impedance of the differential amplifier 159 is characteristically low, within the criteria outlined above.

In Figure 13b, the same circuit is utilized except that the input signal and reference are reversed.

That is, the voltage varying input signal is now applied directly to the non-inverting input of the amplifier 159 while the reference (such as a ground potential connection) is connected through a portion of the resistor R1 to the inverting input of the amplifier 159 with the high input impedance amplifier 161 interposed therebetween. In the case where it is a reference voltage level to which a current drawing input of a circuit is to be connected, rather than a voltage signal, the high impedance amplifier 161 can be omitted if the reference line is either hardwired to the reference potential or of a single pass transistor switch of a uniform and controlled impedance is employed. This is to be compared with connection of an input signal terminal where the number of pass transistors or other types of switches will vary from connection to connection. If the single reference voltage path transistor impedance is known, that is in effect considered part of the input portion of the resistor R1 and the high impedance amplifier 161 can then be omitted. However, it is generally preferable to include the amplifier 161, particularly when pass transistor types of switches are utilized in order that their impedance need not be carefully controlled and the processing tolerance is thus relaxed in order to improve yield and reduce the cost of the individual chips.

Referring to Figure 13c, a simple comparator is illustrated, utilizing the amplifier 159 and nothing more. In Figure 13d, such a comparator with a hysteresis feature is illustrated.

Each of the circuits of Figures 13a-d can be made to constitute a cell, as it is shown, within separate functional modules. It is preferable, however, to combine into a single module cell a circuit that is programmable

in a manner to implement any of the four functions of the circuits just described. Such a cell is shown in Figure 14 where the circuit elements of Figures 13a-d are utilized. Four switches are added in order to allow programming of the function of the module cell, these switches being indicated by numbers 163, 165, 167 and 168. The switches are set in response to configuration data maintained in the configuration register of the module in which the cell is being utilized, the configuration register circuit 45 of the functional module 25 (Figures 1C, 2 and 5) being illustrated as an example. Four functions are selected by these switches, either a positive gain amplifier, a negative gain amplifier, a simple comparator or a comparator with hysteresis. The position of each of the switches to provide these functions is indicated on Figure 14.

In addition to setting the positions of the switches to select the function to be performed by the circuit of Figure 14, it is usually desirable to be able to control certain operating parameters of the amplifier 159. One such operating parameter is the bias current supplied to the amplifier 159. This current can be maintained as low as possible consistent with the desired speed of operation of the amplifier, thus reducing the power consumed by the circuit. Further, the center tap position of the resistor R1 is adjustable by the configuration data loaded into the configuration register 45.

Another programmable voltage mode circuit is illustrated in Figure 15. This circuit will add or subtract signals at its inputs 169 and 171, depending upon the position of switches 173 and 175. Isolation amplifiers 177 and 179 are inserted in the respective

input signal paths 169 and 171 before the inputs of a differential amplifier 182, in order to provide a very high impedance input for the reasons discussed above. A third high impedance input amplifier 181 may be inserted in a reference voltage path that includes a portion of a resistor, depending upon the connection to the reference source, as discussed above. In addition to controlling the position of the switches, the configuration data loaded into the register 45 can be used to control the center taps of the resistances R2 and R3, as well as operating parameters of the amplifiers 181 and 182.

Each of the circuits illustrated in Figures 13-15 includes a programmable tapped resistor, although, in some cases, fixed resistors may be utilized instead. One specific way to program the position of the center resistor tap is shown in Figure 16 where a center tap 183 is selected by closing one of the switches indicated in response to configuration data stored in the module's configuration register 45.

Although two specific programmable function voltage mode circuits are illustrated with respect to Figures 14 and 15, numerous other such circuits with different analog voltage signal processing functions can be provided by using the same approach in combining single circuit functions to form the multi-function circuits of Figures 14 and 15. It is generally desirable to include as many functions as possible in each of the functional modules of the system of Figure 1C, consistent with economical constraints, in order to maximize the flexibility of the types of systems which can be built from a single integrated circuit chip 11.

Each of the functional modules of the system of Figure 1C, those of Figures 14 and 15 being examples, is

designed so that when an input signal is received, a stable, properly functioning circuit is obtained for any of the allowed programmable choices. This is best done by making the analog circuit within each functional module complete enough to form an amplifier, comparator, etc., but with some very well defined programmable internal connections that allow a user to select among different operating parameters. This does not require that two or more different functions be selectably provided in each module (although this is also desirable), which is the case in the examples of Figures 14 (amplifier an comparator) and 15 (adder and subtractor), but rather that any one such function be completely provided within the module for any of the programmable choices. Although this discussion emphasizes such active circuits, the same considerations apply to passive circuit modules such as those which can be formed primarily entirely of switchable capacitor or resistor networks.

This aspect of the present invention may be contrasted with a more generic approach to the functional modules, wherein a large number of transistors are included with a complex switching network that allows the transistors to be interconnected in hundreds or thousands of different combinations. Such an approach allows the user to interconnect the transistors in unworkable combinations, and, even with workable combinations, can result in intolerable levels of parasitic circuit elements. These undesirable characteristics are avoided with the present invention. The present invention should also be contrasted with another approach of providing each module with only part of what is needed to form a functional amplifier, comparator, etc., two or more such modules being necessary to provide the function.

Contrary to these other design possibilities, the functional modules of the present invention cannot be programmed to be unstable, non-functional or have such a high level of parasitics, even if the user is unskilled in analog circuit design. The user needs to possess enough skill to make the right choices in configuring and interconnecting various modules to obtain an overall desired result but does not need to be able to form stable and functional basic analog circuit building blocks from individual transistors and other primitive elements. Such modules are already provided to the user.

Three possibilities are illustrated in Figures 17a, 17b and 17c for circuits within the input module cells that interface with voltage signals outside of the system of Figure 1C. One of these three possibilities is desirably included in each of the input module signal paths. Other circuits, such as filters, amplifiers, and the like, can be included as well, as discussed above with respect to the input modules 27 and 33 of the system of Figure 1C.

The usual voltage signal of an electronic system in which the integrated circuit chip containing the system of Figure 1C is to be used is single-ended. That is, it varies from ground potential (zero volts) to a maximum of nearly the power supply voltage, such as the standard five volts power supply. An example waveform 185 is shown in Figure 17a. The circuit modules of the chip 11 could all operate in the same manner except that any negative going signals then require a second power supply of minus five volts in order to accommodate this. Therefore, it is preferable to convert the single-ended voltage input into a signal that can represent both positive and negative

analog signals within a voltage range of a single power supply, such as five volts.

One such technique is illustrated in Figure 17a wherein appropriate circuits 187, as part of an input module, generate a non-inverted output signal with a reference of a mid-point voltage of the power supply, 2.5 volts in the case of a five volt supply. The signal then varies between this reference and the maximum power supply voltage. As negative signals are generated by inverting these positive signals, therefore, they will extend between the 2.5 volt reference and zero volts. Indeed, such an inversion can take place in the input module, this being shown in Figure 17b as being generated by an inverting input circuit 189.

As an alternative to shifting the reference level and scaling the signal, as described through respective Figures 17a and 17b, a true differential signal can be generated from an single-ended input, as illustrated in Figure 17c, with use of an appropriate conversion circuit 191. Such a circuit generates in two output lines 193 and 195 replicas of the single-ended input but with opposite polarities. That is, a line 193 can generate a scaled version of the signal that always extends from 2.5 volts to 5 volts while generating in a line 195 an inverted signal extending from the 2.5 volt reference to zero volts. The differential signal is generally preferred since either an inverted or non-inverted form of the same signal is readily available at all points in the circuit. However, it has a disadvantage that a pair of conductors needs to be extended everywhere through the circuit rather than a single conductor with use of a common reference. When differential signals are utilized, the individual signal paths within the bus 41

are formed of two conductors, rather than a single conductor for other types of signals described above.

If one of the input voltage conversions of Figures 18a, 18b or 18c is utilized, this conversion is reversed in each of the output modules of the system of Figure 1C. In such a case, a corresponding one of the conversion circuits of Figures 18a, 18b or 18c is utilized at the output. That is, if the circuit 187 of Figure 17a is used in the input modules, the conversion of a circuit 197 of Figure 18a is used in the output module. A similar correspondence exists between the input conversion 189 (Figure 17b) and the output conversion 199 (Figure 18b). When a two-wire, fully differential signal is used on-chip, the input circuit 191 (Figure 17c) and output circuit 201 (Figure 18c) are used. Any one of the illustrated conversions generates output signals in the usual form, having a swing of from zero volts to some positive voltage such as five volts. In any event, the signal format at the output is made to be the same as that received at the input.

In describing the input and output signal conversion circuits of Figures 17 and 18, it has been assumed that the circuit chip being described is designed to be used in a normal analog system where single ended voltage signals are used. However, it will be recognized that almost any type of conversion can be made at both the input and output modules in order to be able to use on the chip the most appropriate signal format for a given application while remaining able to communicate outside the chip in some other signal format that exists in the user's system. The user can even use current signals, so conversion into and out of a specific on-chip voltage signal format is then required.

Conversely, current signals can be used on-chip, as described in the next section, so conversion into and out of a user's different current signal format may be required. And if the user's system uses voltage signals, a conversion into an on-chip current signal format is made in the input and output modules.

The voltage mode circuits of Figures 13-16 are designed to operate with continuous varying voltage signals. However, circuits operating in a charge mode could be used instead, depending upon the specific application to which the circuit chip is to be put. Examples of appropriate circuits which implement the system of Figure 1C with charge mode (switched capacitor) modules are given below in another section.

Current Mode Operation

As another possible implementation of the configurable analog system of Figure 1C, the functional modules thereof may process the analog signals in a current mode. For many applications, current mode analog module cells can be simpler than their voltage counterparts since high bandwidth, high gain operational amplifiers with feedback are not required as they are in the continuous voltage mode and discontinuous charge mode systems. Further, current mode circuits have a much lower sensitivity to electromagnetic interference because of predominantly low impedance nodes that are utilized.

With reference to Figure 19, the criteria of current mode modules which allows them to be interconnected is given. Two current mode cells 211 and 213 are shown connected together through interconnection circuits 215 that include at least one signal path of the bus 41, and one or more pass transistor or other types of

switches or interconnections that each provide some level of impedance. In order to be insensitive to the variable impedance that interconnect the cells, each current mode module cell is made to have a very low input impedance and a very high output impedance. That is, the input impedance of each cell is made to be very low with respect to the lowest possible expected interconnection impedance between cells, at least one tenth of that expected interconnection impedance or lower. Similarly, the current mode module cell output is made to be very high with respect to the largest expected impedance of the interconnecting network, preferably one hundred times or more higher.

Referring Figure 20, a current amplifier 245 has current signal inputs in conductors 241 and 242, and current signal outputs in conductors 247 and 249. Such an amplifier can be employed as one or more of the current mode cells within a module of the system of Figure 1C, or as a core of one or more modules. An example circuit for the current amplifier 245 is shown in Figure 21 and described below. A fully differential current output is provided in lines 247 and 249. Since is usually preferable to communicate over the bus 41 (Figure 1C) between modules with fully differential current signals, such a signal is applied to inputs 241 and 242. However, a single ended current signal may be used and, in that case, is applied to only one of the inputs 241 and 242, the other remaining unconnected. The fully differential output results, in the embodiment of Figure 21, when the input is either also fully differential or is single ended. Control signals are applied through circuits 244 from the configuration register and decoder of the module in which the amplifier 245 exists. These control signals

set operating parameters of the amplifier, including its gain and bias currents. Other components are combined with the current amplifier in order to provide modules that perform other functions. Modules may be so formed to act as a signal rectifier, filter and comparator, for example. Operating parameters of such modules are made selectable by the individual module configuration data. Further, these and other functions may be combined into a single current mode module whose function is selected by configuration data loaded into its configuration circuits.

Although the processing within the integrated circuit chip of Figure 1C can be done totally in a current mode, other circuits with which the integrated circuit chip is to be used will generally operate in a continuous voltage mode. Thus, the input and output modules of the circuit of Figure 1C need to convert the signals between voltage and current modes. Figure 21 shows and example conversion circuit within each of the input modules 27 and 33. An operational amplifier 343 acts as a buffer to receive a voltage input signal in a line 345 and apply it to a gate of a transistor 347 connected in series with a resistor 349 between the voltage sources. The source-drain current through the transistor 347 is thus proportional to the input voltage. This current is then mirrored into a second transistor 351, whose single ended output in a line 352 is used internally in the system of Figure 1C. For a system having fully differential internal signal paths, another circuit like that of Figure 21 is added, this second circuit having the opposite type of transistors 347 and 351.

A reverse conversion is then provided at the signal outputs of the output modules 37 and 39 of the system of Figure 1C. Two such circuits for doing so are

illustrated in Figure 22a or 22b, depending upon whether a non-inverting or inverting voltage signal output is respectively desired. The circuit of Figure 22a includes a differential amplifier 353 receiving a current signal in a line 355, through a resistor 357. The voltage developed across the resistor 357 is applied to a non-inverting input of the amplifier 353, while its inverting input is connected to a signal output 359. Similarly, the circuit of Figure 22b uses a differential amplifier 361 with a current signal input being received in a line 363 through a resistor 365 that is connected to the signal output 367. A voltage drop across the resistor 365 is applied to an inverting input of the amplifier 361, while its non-inverting input is connected to ground potential. In systems where the internal signal paths are in fully differential form, the selected circuit of either Figure 22a or 22b is duplicated with the differential amplifier of the added circuit being connected with its input polarities being reversed.

Charge Mode Operation

The basic mode of operation of known charge mode circuits is the transfer of packets of charge from capacitor to capacitor by use of appropriate repetitive switching. The charge level transferred at a particular instant is proportional to the value of the voltage signal at that time. This charge mode technology is desired for many applications because of its precision but presents additional considerations when implemented in a configurable analog module circuit of the type being described.

When the charge mode is internally used, the input and output modules of the system of Figure 1C are

caused to convert between discontinuous charge levels used in the functional modules and the usual continuous signals of the user's system with which the chip is to be used. The input modules periodically sample an incoming continuous voltage signal and provide successive output levels of charge that are proportional to corresponding voltage samples. The input signal is usually low pass filtered in advance of being sampled, in order to avoid aliasing. The output modules do the reverse, namely convert successive charge levels received at their inputs into a continuous voltage signal as the output of the circuit.

With reference to Figure 23, it will be noted that the input and output impedance constraints are the same as those for voltage mode operations as described with respect to Figure 12, with the addition of a very low effective input capacitance as a desirable characteristic. An output of one charge mode cell 395 is connected through interconnection circuits 397 to an input of another charge mode cell 399. Figure 24 shows an example of a circuit that can be used as the cell 127 of the functional module of Figure 5. The Figure 24 circuit is a variable gain amplifier which meets the input and output constraints illustrated in Figure 23.

The circuit of Figure 24 includes an amplifier 401 having a variable input capacitor C1 and a feedback capacitor C2 extending from an output to its inverting input. Two switches 403 and 405 are respectively provided in series with the capacitor C1 in the input circuit and across the capacitor C2 in the feedback circuit. The switches 403 and 405 are synchronously switched in response to two active clock signals $\phi 1$ and $\phi 2$ from a circuit 407. These two clock signals are 180° out of phase

with each other and cause switches 403 and 405 to switch simultaneously between their indicated respective positions 1 and 2. When these switches are in their position 1, when the clock phase $\phi 1$ is active, the switches cause the input capacitor C1 to be charged to a value proportional to an input voltage in a line 409 with respect to a reference signal in a line 411. In the next part of the cycle, when the clock phase $\phi 2$ is active, the switches 403 and 405 are moved to their indicated positions 2, thereby connecting the input capacitor C1 to the reference line 411 and removing the short across the feedback capacitor C2. This causes charge to be transferred from the capacitor C1 to the capacitor C2. The cycle is then repeated by moving the switches back to their position 1, and so forth. The gain of the Figure 24 amplifier circuit is determined by a ratio of the values of the capacitors C1 and C2, just as if resistances were being used in place of the capacitors in a continuous voltage mode circuit.

The gain of the amplifier circuit in Figure 24 is programmed by adjusting the value of the capacitor C1 from a functional module configuration data stored in its configuration register 45. The variable capacitor C1 is preferably implemented by use in a number of fixed capacitors in different but related values which are combinable by operation of various switches to provide a range of capacitance in incremental steps. The configuration data for a charge mode functional module cell also contains one bit of data which controls, through a line 413, the phases of the switch controlling clock signals. That is, a control signal of the line 413 controls, through circuits 207, the absolute phases of the $\phi 1$ and $\phi 2$ clock signals. The purpose of this is to

permit adjustment of the signal sampling phases for proper coupling of signals between charge mode modules as described below.

In order to charge the input capacitor C1 when the switch 403 is in its position 1, current flows in the input line 409. Since this violates the high impedance criteria established for voltage mode modules, a high input impedance buffer amplifier 415 is inserted in the path of the input signal so that the circuit of Figure 24 satisfactorily operates as a functional module in the system of Figure 1C.

Referring to Figure 25, a single example of the operation of the circuit of Figure 24 is given. An input voltage 417 is effectively sampled at a rate determined by the clock signals $\phi 1$ and $\phi 2$, to result in an output signal 419. It will be noticed that the output signal, corresponding to the charge stored in the capacitor C2, follows the input voltage 417 during the half of the clock switching cycle where the switches 403 and 405 of Figure 24 are in their position 2. The output is thus valid when the clock signal $\phi 2$ is active. When in position 1, the switch 405 shorts out the capacitor C2 thereby discharging it, and causes the output signal of the amplifier 401 to fall to the reference level voltage in the line 411. This is commonly referred to as a "return-to-zero" (RTZ) signal, since the reference represents the zero level.

Because of this RTZ form of output signal 419 from the type of charge mode module being described, the phase of switching operation of adjacent modules must be coordinated. With reference to Figure 26, a first functional module 425 of a type including a charge mode cell of Figure 24 is coupled to another such module 427 through a portion 429 of the signal paths and switching

network. The relative phase of operation of the modules 425 and 427 is set by the PI configuration signal in each module to bring about this phase relationship. This is necessary since, as can be seen from the discussion of Figure 24, the input signal of a module such as module 425 is sampled at $\phi 1$ and presented at its output in the next half clock cycle $\phi 2$. The second module 427 must then sample that output, which is presented as its input, at the time $\phi 2$. Obviously, as can be seen from the output signal waveform 219 of Figure 25, a sampling at $\phi 1$ would provide a zero voltage and totally loose the signal being processed. By alternating operational phases of adjacent modules, the second module 427 samples that output signal when it is high, in between periods that it is returned to zero or some other reference potential.

The direct coupling of RTZ format signals between modules by use of this relative phase control has a significant advantage. The usual technique is too smooth, by use of a sample-and-hold circuit or otherwise, the output signal 419 (Figure 25) so that it approximates the shape of the input waveform 417. However, this does introduce some degree of distortion of the signal and, if done at the output of each of the functional modules of the system of Figure 1C, would accumulate significant amounts of distortion in the overall operation of the illustrated integrated circuit. The ability to directly communicate RTZ signals between modules eliminates this source of distortion and a considerable amount of circuitry as well. The RTZ signals need to be smoothed and converted to continuous voltage mode signals only when they are outputted from the chip.

Another use of the switching phase control of the charge mode functional module cells described above is

illustrated in Figure 27. The charge mode amplifier circuit 431 can be used to sum two RTZ signals in lines 433 and 435 if they are in phase with one another. As an illustrative example, the signal path developing the signal 433 includes a single functional module of 437, and a portion 439 of the interconnecting network, while the branch developing the signal 435 includes two such modules 441 and 443, connected together by portions 445 and 447 of the interconnecting network. The relative switching phases of the input modules 437 and 441 are set by the respective PI configuration signals to be of opposite phase so that the signals in lines 433 and 435 are in phase. This avoids the necessity of inserting a one-half cycle delay in one of the inputs to the summing amplifier 431 to compensate.

Referring to Figure 28, an output module of Figure 6 is illustrated for the charge mode case. A RTZ form of voltage signal obtained by appropriate switch connection of a line 451 with a signal path in one of the bus 41 is applied to a sample-and-hold circuit 453. The input signal is caused by phase control circuit 455 to be sampled during periods when it represents the value of the signal, and not during periods when the signal has dropped back to its zero or other reference level. One of the two possible phases of operation is selected by the output modules configuration data in the register 53. The sample and hold output is then passed through an optional smoothing filter 457 and a driving amplifier 459 to provide an output signal in a line 461 that goes directly to an output pin of the integrated circuit.

Referring to Figure 29, an input module of type illustrated in Figure 4 is shown for the charge mode case. A continuous voltage signal input from a pin of the

integrated circuit is applied by a line 463 to a low pass filter 465 whose characteristics may optionally be programmable by a portion of the configuration data stored in the register 43. A buffer amplifier 467 has an output in a line 469 that is a continuous voltage signal adapted for application to an input of an RTZ charge mode module through a portion of the interconnecting network. The low pass filter 465 is set to have a cutoff frequency that eliminates all frequencies of the input signal on the line 463 that are higher than one-half the sampling frequency of the signal in the RTZ modules. This prevents false sampling and aliasing during the sampling process. In cases where it is desired to make that sampling frequency programmable, the filter 465 can be made to have a programmable cutoff frequency that is set by data in the configuration register 43.

Additional System Features

The system described above, as shown in Figures 1C-3B, is easily reconfigured, even during normal operation of the circuit chip. Three principal features described above contribute to this ease. One feature is the addressability of individual module shift and configuration registers, so that the entire bit stream does not have to be reloaded each time that one or a few bits are desired to be changed. Additionally, this feature allows the shift register of a module that is not included in a particular system configuration to be bypassed during use of that system, thereby reducing the number of bits in the serially combined shift registers. In complicated systems, the overhead required for individual register addressability can make it desirable to form adjacent registers of two or more modules into

groups that become the smallest sub-set of the serially connected registers that may be individually addressed. This still provides a significant advantage. In simple systems, individual fields within the configuration register of a single module can even be made to be separately addressable.

It is even quite useful, in the system of Figure 1C, if only the configuration registers in the input module 33 and test probe module 110 are separately addressable, all other module registers being programmed together by a single configuration bit stream. This allows the input multiplexer of the input module 33 and the internal node to which the test probe output 112 is connected to be easily changed as part of the operation of the circuit system. Since the need to change the configuration of the other modules is less frequent, this minimizes the extra overhead required for the individual addressability.

The second feature which makes it easy to reconfigure all or a portion of the circuit chip is the use of a command byte or bytes 85 (Figure 3A) which are decoded by the decoder 89 (Figure 2) in order to either determine how any following data 104 is to be used, or to directly execute the command without handling other data. An external controller, if being used with the circuit chip during its operation, communicates such commands and data in a single serial data stream. The commands are communicated into the circuit chip over the same path as the configuration data, through a single pin.

The third feature contributing to the ease in reconfiguring the circuit chip is the result of using both shift registers and configuration registers in the various modules, as shown in Figure 2. It is the shift registers

which are connected into a single serial register circuit. Configuration data which controls a module at a given instant is that which is stored in its separate configuration register. This allows new configuration data to be loaded, either for the entire chip or a separately addressable portion of it, into the shift registers without disturbing operation of the circuit. It is only when the load signal is issued in line 70 that the new configuration data gets moved into the configuration registers to control operation of the circuit. The change to new configuration data is thus accomplished very swiftly.

Another feature may also be included to further increase the flexibility of configuring the circuit chip. Referring to Figure 30, configuration circuits 43' of an input module 33', corresponding to configuration circuits 43 of the input module 33 of Figures 1C and 4, include added registers for storing more than one set of configuration data. Usually, only different sets of certain fields of the configuration data are stored in the individual modules. Four such sets are stored in the example of Figures 30 and 31, but any number of two or more is possible. Such a configuration circuit then also includes a switching circuit to enable the user to choose which of the stored sets of configuration data are to be used at any one time. In addition to the input module 33', the same feature is shown for configuration circuits 45' of a functional module of the system. This feature may be included in any number or all of the input, functional and output modules of the system of Figure 1C.

The example circuit 43' of Figure 30 include series connected configuration circuits 635, 643, 647, 657, 667 and 675. The circuits 643, 657 and 675 do not

contain space to store multiple sets of data, so are similar to the circuit 43 described with respect to Figure 2, as shown for the circuit 643 in Figure 31. However, the circuits 635, 647 and 667 do have that capability, so a switching circuit is provided in conjunction with each of them in order to select one of the stored sets of configuration data for use at a time.

An example of the configuration circuits 647 is given in Figure 31. Four registers 701, 703, 705 and 707 are connected in series in the system configuration data path. A separate set of data can be stored in each of these registers for controlling the gain and/or other operating parameters of an input amplifier 631 within the input module 33'. In response to a system load signal in a line 70, this data is latched into corresponding configuration registers 709, 711, 713 and 715. The data of one of these configuration registers is selected by a multiplexer 649 in response to a control signal in lines 665. The selected configuration data is decoded by a decoder 651 in order to provide control signals in lines 653 to the amplifier 631. Configuration circuits 635, 637, 639 and 667, 669, 671 are similarly implemented, as are circuits 693, 695, 697 of the functional module register 45'. In addition to providing multiple data for individual operating parameters, the same technique is employed to allow a rapid change between module functions and/or interconnections.

There are many arrangements which can be used to control the selection of the multiple sets of configuration data that is made available by the system modification shown in Figures 30 and 31. Each of the selecting multiplexers 637, 649 and 669 of the input module can be operated independently, in response to

separate control signals, to control, respectively, operating parameters of the filter 125', the amplifier 631 and an offset bias source in the form of a digital-to-analog converter 633. An output of the offset 633 is applied to a second input of the amplifier 631, and is thus added to the signal input from the filter 125'. The multiplexer control signals are shown in the example of Figure 30 to originate from a channel decoder circuit 655 through respective lines 663, 665 and 679.

However, it is generally adequate, and often preferable, to switch all of the multiplexers 637, 649 and 669 together. The result is then to allow operation of the input module 33' with a number of different configurations equal to the number of multiple shift registers provided, in this case four. The parameter(s) controlled from the register 643 remain the same when any of the four selections is made.

The decoder 655 responds to any one of three switching control inputs, thereby allowing the input channel and module configuration to be selected by any one of the three control signals. A first of these control signals comes from the one field of configuration data stored in the configuration circuit 657, through lines 659. A second control signal is supplied from external pins through lines 84. A third control signal is available from a sequencer 656 over lines 658. One field of the configuration data loaded in the circuit 657 selects one of these three signals to sequence the channel decoder 655 at any given time.

The sequencer 656 is preferably a state machine which steps through a predefined sequence, that sequence optionally being alterable at certain points by the value of at least one signal input 660. The signal in line 660

can be obtained, for example, from a temperature sensor that is either internal to the chip or provided externally. This allows operation of the chip to be altered as its operating temperature changes. Alternatively, the signal input 660 can be derived from the value of a signal elsewhere on the chip.

The input multiplexer 124' can also be operated under control of the decoder 655 in a manner to provide a specified set of operating characteristics for each of the inputs 13 to the input module 33'. That is, when the input line multiplexer 124' is caused to connect one of the input lines 13 through the filter 125' to the amplifier 631, the multiplexers 637, 649 and 669 are also switched to positions predetermined by the structure of the decoder 655. This provides a particular set of operating parameters for these components and a specific value of offset voltage from the bias source 633, all in response to data which has been loaded into the particular ones of their multiple configuration registers that have been selected.

The decoder 655 is usually configured to switch all of the multiplexers 637, 649 and 669 together, thereby providing four different sets of operating parameters, in this example. If there are also four inputs, each different input signal is provided with a differently configured input module. If there are more than four inputs, the same operating characteristics will be provided for more than one input. Alternatively, the decoder 655 may be configured to switch each of the multiplexers 637, 649 and 669 independently, thereby providing a much larger combination of operating parameters which can be shared among the inputs.

In addition to controlling the input module 33', the decoder 655 may also control the multiplexer 695 of a functional module through lines 687, that of another module through lines 689, and so forth. This allows any number of the modules of the circuit chip to be configured in a specified manner for each of the input signals 13. Of course, these other modules can, alternatively, have their stored configuration data selected independently of the selected input signal. This multiple configuration register technique can also be applied to field programmable gate arrays (FPGAs).

In the example being described with respect to Figures 30 and 31, only internal operating parameters are being controlled by the various alternate configuration data fields. The function of some of the individual modules may also be controlled, such as changing from a simple buffer to a comparator, for example, during operation of the circuit, particularly if done simultaneously with switching between input signals. Similarly, alternate configuration fields may be provided for changing the specific interconnections between at least some of the modules. One advantage of the switchable input multiplexer 124', when combined with the ability to select a unique configuration of the rest of the circuit for each selected input, is that a single circuit chip can be time shared with several different signals. Alternatively, a single input signal can be connected simultaneously to two or more of the input lines 13 so that the different circuit chip configurations are used with the single signal. Indeed, if it is known that the circuit chip is only to be used with a single input signal, the input multiplexer 124' can be omitted while the easy reconfigurability feature is retained.

It will be recognized that certain detail of the configuration circuits 43 of Figure 2 has been omitted from the circuits 43' of Figure 30. It is contemplated that the individual addressability of the configuration circuits 43 also be included within circuits 43', although not required. In such a case, a counterpart to the bypass path 101 (Figure 2) is also included as part of the configuration circuits 43'. A combination of the features of being able to independently address various segments of the series connected registers, the storage of alternate configuration data in individual modules, when desired, and the ability to load new configuration data in the background while the system is operating combine to maximize the configurability of the circuit chip for a wide variety of applications.

Referring again to Figure 30, a circuit to correct for signal offset errors is illustrated for inclusion in the circuit chip. Calibration logic 681 causes the voltage of the offset source 633 to be adjusted according to a given sequence. This sequence is initiated when either an external trigger signal is applied in a line 683 or a specific command 85 (Figure 3A) is given through the serial configuration data input 69 (Figures 1C and 2). The offset adjustment sequence is terminated when the logic 681 receives a signal in a line 682. The signal line 682 can be connected through an external pin (not shown) to an output pin of the circuit chip in order to be connected to one of signal outputs 15, 17 or 19 (Figure 1C). Alternatively, as shown in Figure 30, this connection is made on the chip itself, the line 682 being connected to an output of a comparator 685 which has its inputs connected to one or more chip output lines 15, 17 or 19 by a multiplexer 698, as shown, or to any other node

within the circuit chip. The multiplexer is controlled by a signal in a line 696 from a configuration register stage 694. The comparator 685 is enabled by an external signal in the line 683. One use of this offset adjustment capability is to eliminate any d.c. bias of an external signal applied to the chip so that such a signal may be directly coupled with the chip without the need for the use of an external capacitor.

This allows the auto-zeroing of any of the outputs 15, 17 or 19, as selected by the multiplexer 698, with any of the inputs 13, as selected by the input multiplexer 124'. During the auto-zeroing operation, one of the output modules 37' and 39' being used is temporarily reconfigured into a simple amplifier of unity gain. This is accomplished in response to a control signal from the calibration logic 681 in one of the lines 684 or 686. After the auto-zeroing operation is concluded, the temporarily reconfigured output module is allowed to revert to a configuration that is specified by the data in its configuration register.

As is typical of analog circuits generally, those of the individual modules being described herein can experience errors, because of manufacturing variations and/or drift over time, in their gain, offset, and the like. It is therefore desirable to be able to remove such errors through calibration. Calibration is traditionally executed by applying a known signal to the input of a circuit which is similar to an expected signal when the circuit is to be used, and then adjusting some characteristic of the circuit to obtain a desired output. However, the reconfigurability of the system being described, particularly that of its individual modules, allows the analog path to be calibrated by using a more

convenient standard input signal and then adjusting the circuit to obtain a different than the expected normal output. For example, if it is desired to configure a functional module of an amplifier with negative gain, that module can be temporarily reconfigured to function as an amplifier with positive gain. An offset voltage is then adjusted within the module while an input signal is applied, in order to remove any offset of the amplifier, while monitoring an output for an expected signal from a positive gain amplifier. The module is then reconfigured back to its original amplifier with negative gain, having thus been calibrated.

A single such calibration of a module can often serve to calibrate the module for operation in any of its configurable functions. Another example is to calibrate a module, such as one of the output modules 37 and 39, to be configured as a comparator by temporarily configuring it as a linear amplifier, such as use of a signal in the appropriate one of lines 684 and 686. This temporary configuration is made responsive to a configuration control signal on the pin 683 (Figure 30) or a command 85 (Figure 3A). Any offset of the linear amplifier is then removed by adjusting an offset shifter or other similar means, and then configure it back to function as a comparator, which is now offset free. Yet another example is in the calibration of a filter, such as the center frequency of a bandpass filter, by reconfiguring the circuit as an oscillator and then calibrating the oscillator against a known reference clock, after which the circuit is reconfigured back into a filter which is now calibrated.

As a variation in the configuration systems described above, a configuration register in a module may

be replaced by, or supplemented with, a counter that has an initial value loaded from its associated shift register but which can be numerically incremented or decremented by a desired amount with a separate control signal. Such a control signal can be derived from the configuration control circuit 63 (Figures 1C and 2) in response to appropriate configuration data (Figure 3). This allows a limited change in the content of a configuration register without having to reload its associated shift register with new data. This is particularly useful for configuration register fields which contain numeric data that set a level of some type, such as when used to set an analog bias or reference level through a digital-to-analog converter (DAC) that receives the configuration register field data as an input. The reference voltage sources 139 and 140 (Figure 6) of an output module can be controlled this way, as can the offset source 633 (Figure 30) of an input module. The counter technique is particularly advantageous when a frequent adjustment is required during use of the analog system.

Figure 32 shows a test probe circuit for the module 110 of Figure 1C, as an alternative to that of Figure 7. In addition to configuration circuits 111' controlling the connection of an input of amplifier 130' to a certain one of the bus circuits 41, operating parameters of the amplifier 130', such as gain, may also be controlled through lines 724 from one or more bits of the configuration data loaded into the test probe module 110. In addition to the signal bus lines 41, other analog signal points within the circuit chip may be accessed through a multiplexer 726 and one or more additional lines 728 that provide inputs to the multiplexer 726. Certain of the lines 728 can be connected to other signal carrying

nodes internal of various of the input, functional and output modules. Others of the lines 728 can be connected to other types of analog signal points within the circuit chip, such as voltage references. An output 729 (Figure 1C) of the bias generator 113 is an example of such an internal reference voltage that may be connected to an external pin through the test output line 112'.

It is also important that the input characteristics of the amplifier 130' be such that it does not affect operation of the circuit chip by its connection to an internal node. For voltage mode circuits, an impedance of the input to the amplifier 130' in excess of at least 100 times that of the outputs of the circuits driving the nodes is desired, within the frequency range of operation of the circuit.

It is usually desirable to also have access to some of the digital signal paths within the chip. Therefore, the test probe circuit of Figure 32 includes a second multiplexer 721 for connecting, in response to the contents of lines 723 which are driven by a configuration data field, an input of a buffer amplifier 725 to one of several digital signal paths on the circuit chip. An output of the amplifier 725, when enabled by a signal in a line 727, is connected to an external pin through the test module output line 112'.

One desirable input to the multiplexer 721 is the configuration data which is stored on the chip in a few or all of its configuration registers. Lines 722 (Figures 1C and 32) are connected as an output of the last configuration circuit 72 to allow the configuration data to be shifted out of the shift registers, through the multiplexer 721 and amplifier 725, to the test module output line 112'. Less than all of the shift registers

may be read by bypassing others in the same manner as described above with respect to Figure 2. Prior to this reading step, the data in the desired configuration registers is written in parallel into corresponding ones of the shift registers, in response to an internal "unload" control signal that is generated in response to an appropriate command 85. As this configuration data is shifted out of the serially connected shift registers, it can also be looped back into the chain of configuration circuits through the lines 55 so that the contents of the shift registers at the end of this read-out cycle are the same as at the beginning. After this cycle is completed, the data in the shift registers is again loaded into the corresponding configuration registers. During the cycle, the configuration data appears in line 112' in the form of a serial data stream, and thus may be captured by a host computer system to enable the user to review how a specific circuit chip has been configured. This is accomplished without affecting operation of the circuit, since the data in its configuration registers is not disturbed. A system controller can then periodically review the contents of some or all of the configuration registers in real time, without disturbing operation of the circuit.

The configuration data stored on chip in the memory 73 may also be read out through the line 112' by connecting the lines 74 as an additional input to the multiplexer 721. Another input can be connected to the output 730 of the clock oscillator 75. Yet another input 731 can originate from the configuration control circuits 63 to allow monitoring whether a command is received and properly processed. Further internal digital signal nodes may be similarly made to be accessible through the test

module output pin, an example being a node within the power down circuitry.

A configurable analog circuit chip according to the preceding discussion is often used as part of a larger system that includes a system controller. This is schematically shown in Figure 33. A configurable analog chip 735 receives one or more input analog signals from some source 737 and delivers one or more output analog signals to a circuit 739 which utilizes them. A controller 741, including a microprocessor, operates a digital control portion of the system, providing the configuration data for the circuit chip 735. Since the circuit chip 735 allows dynamic changes to be made in at least certain fields of the configuration data, the controller 741 can update one or more configuration data fields during operation of the chip 735. This ability can be used, as shown in Figure 33, to form a closed loop control system wherein an output signal of the chip 735 is digitized by an analog-to-digital converter 740 for use by the controller 741. The controller is then programmed to monitor some characteristic of the output signal, such as its level, and to change some aspect of the operation of the circuit chip 735, such as the gain of an amplifier in one of the modules, in order to maintain that characteristic of the output signal within a predefined range. The ability to reprogram less than all of the configuration data fields and the use of both shift and configuration registers allows the circuit chip 735 to be so used.

Another control technique which may be implemented by the configurable analog chip alone is illustrated in Figure 34. A chip 745 is internally configured with one or more of its modules providing a

signal to control others of its modules which form the signal path from the analog signal input to its output. In Figure 34, the chip of Figure 1C is configured with the input module 33' (Figure 30), one or more of the functional modules 21, 23 or 25, and the output module 39 forming the desired analog circuit. The switching signal on the lines 84 (Figure 30) is developed by a connection together of the input module 27 and the output module 37. The output 15 is connected by an external wire circuit 747 to the switching control input 84. Optionally, the circuit connection 747 can be included internal to the circuit chip.

In operation, some characteristic of a signal applied to the input 11 of the circuit chip 745 (Figure 34), such as its level, is used to generate a signal output 15 that switches the input signal and circuit characteristics of the input module 33' in response. The output module 37 is used to generate a binary output having a level that depends upon whether the level of the input signal 11 is above or below some threshold level. In one specific application, the input 11 receives the same signal as applied to one of the input lines 13, so that the circuit configuration, such as amplifier gain or signal offset, is changed in response to that input signal going out of a range defined by the configuration of the output module 37. This can be used to provide an automatic ranging function.

Figures 35 and 36 show two different integrated circuit layouts for a type of system earlier described with respect to Figure 1C. All circuit elements for each of the various input, functional, output and other modules are grouped together within the areas indicated in Figures 35 and 36 by the various boxes and labels to indicate

their individual functions. The location of the signal bus 41 is shown cross-hatched, and the configuration circuits are shown distributed around the chip in rectangular boxes which are shown shaded. In Figure 35, each of the configuration circuits is positioned adjacent the modules which it controls with the configuration data stored in them. In Figure 36, the configuration circuits are positioned primarily around the periphery of the circuit chip. In each case, the shift registers of the individual configuration circuits are connected together by conductors shown as heavy lines extending between the configuration circuits.

The layout of Figure 36 has an advantage when a configured circuit chip is to be implemented in a mask programmed version. Once the configuration data is finalized for the programmable version shown, that data may then be implemented by permanent wire connections which replace the configuration circuits. The area of the mass produced chip is then shrunk since the rather bulky programmable configuration circuits are eliminated. In the layout of Figure 36, this leaves a compact mask programmed circuit of smaller overall area than the programmable version.

In each of the layouts of Figures 35 and 36, the various circuit modules are arranged in a pattern that minimizes the overall circuit area, minimizes the lengths of sensitive signal paths, and the like, as is common in integrated circuit layout design efforts. If a much larger number of circuit modules were to be provided on a single circuit chip, such as by the inclusion of many more functional modules, a more regular arrangement of modules may be preferable. The regularity of an array of input,

functional and output modules, such as arranged in rows and columns, would then have some advantages.

As previously referenced, each of the modules on the integrated circuit chip is designed to operate in a stable and predictable manner when any combination of its allowed functional and operating parameters is chosen by the user. Further, the modules and interconnection network are designed so that any possible interconnection of the modules does not disturb such stable operation. The user who is configuring the circuit chip does not, therefore, need to be concerned whether the configuration choices being made will cause the configured system to operate in a stable manner. Once an operating parameter such as gain or offset is selected for a particular module, for example, that characteristic does not change when the module is interconnected in any particular manner with other modules. Similarly, the linearity and phase shift characteristics of individual modules remain the same for the various possible interconnections. This is made to be the case for any selected of the possible functions of the modules. Particularly, undesired oscillation of a module is avoided by maintaining a sufficient phase margin in each under all practical system configurations.

Although the numerous aspects of the present invention have been described with respect to preferred embodiments and examples thereof, it will be understood that the invention is entitled to protection within the full scope of the impending claims.

IT IS CLAIMED:

1. In an integrated circuit chip having a signal input and a signal output, a configurable analog circuit therebetween comprising a plurality of analog circuit modules connectable together in a path between said signal input and said signal output in various arrangements according to interconnection configuration data, at least some of said modules having one or more operating parameters which are selectable in response to parameter configuration data, and at least some of said modules being configurable to perform one of a plurality of analog signal processing functions in response to function configuration data, said circuit chip additionally being capable of storing said configuration data.

2. The circuit chip of claim 1 which comprises a series connected plurality of shift registers extending from a configuration data input for serially receiving said configuration data therethrough.

3. The circuit chip of claim 2 which comprises a plurality of configuration registers which are individually loaded in parallel from individual ones of said plurality of shift registers in response to a load signal.

4. The circuit chip of claim 3 which comprises a plurality of decoding circuits operably coupled with individual ones of said plurality of configuration registers and having decoded outputs coupled to circuit elements controllable thereby.

5. The circuit chip of claim 4 wherein each of at least some of the decoding circuits are connected to at least two of said plurality of configuration registers through a multiplexer to receive configuration data from a selected one of said at least two configuration registers according to a control signal applied to the multiplexer, thereby allowing a rapid change of the configuration data that is applied to at least some of the circuit elements controllable by the decoder.

6. The circuit chip of claim 5 wherein the plurality of analog circuit modules includes an input module having a multiplexer that responds to said control signal to select one of a plurality of external input signals for the input module.

7. The circuit chip of claim 3 wherein the configuration data contents of the configuration registers are loadable into corresponding ones of the shift registers in response to an unload command, and the configuration data in the shift registers are serially read out of the circuit chip in order to ascertain the contents of the configuration registers.

8. The circuit chip of claim 2 which comprises means for decoding and executing commands introduced through the configuration data input.

9. The circuit chip of claim 2 wherein individual ones of said series connected shift registers are addressable by controllably bypassing others of said shift registers.

10. The circuit chip of claim 2 wherein individual ones of said series connected shift registers providing configuration and to one of the modules not being used is bypassed when shifting data through said series connected shift registers.

11. The circuit chip of claim 2 wherein the series connected shift registers are positioned around a periphery of the circuit chip.

12. The circuit of claim 1 which additionally comprises a plurality of signal paths forming a bus, wherein an input or output of at least some of the modules is permanently connected to a unique one of the bus signal paths and the other of the input or output of at least some of the modules is selectively connected to said signal paths in response to said interconnection configuration data.

13. The circuit chip of claim 1 which additionally comprises a test probe module responsive to test probe data introduced through the data input for selecting an internal circuit node for connected with a test probe output of the circuit.

14. The circuit chip of claim 1 which additionally comprises means connected to said circuit output for setting a level of offset to a signal received through said signal input.

15. The circuit chip of claim 1 wherein the plurality of circuit modules operate with current mode

signals, and further wherein a conversion is made in said circuit chip between said current mode signals and voltage mode signals at said chip signal input and chip signal output.

16. The circuit chip of claim 1 wherein the plurality of circuit modules operate with charge mode signals, and further wherein a conversion is made in said circuit between said charge mode signals and voltage mode signals at said chip signal input and said chip signal output.

17. The circuit chip of claim 1 wherein inputs and outputs of the modules which are connectable together are provided with relative impedance characteristics to render operation of the modules substantially insensitive to any of the interconnection configuration data.

18. The circuit chip of claim 17 wherein said plurality of analog circuit modules individually include circuits operating in a voltage mode and which have an impedance (a) at their individual inputs that is ten or more times a highest impedance that can result from interconnection between these inputs and an output of another one of the plurality of modules according to the interconnection configuration data and (b) at their individual outputs that is one-tenth or less of a lowest impedance that can result from interconnection between these outputs and an input of another one of the plurality of modules according to the interconnection configuration data.

19. The circuit chip of claim 17 wherein said plurality of analog circuit modules individually include circuits operating in a current mode and which have an impedance (a) at their individual outputs that is ten or more times a highest impedance that can result from interconnection between these inputs and an input of another one of the plurality of modules according to the interconnection configuration data and (b) at their individual inputs that is one-tenth or less of a lowest impedance that can result from interconnection between these inputs and an output of another one of the plurality of modules according to the interconnection configuration data.

20. The circuit chip of claim 1 wherein the individual modules are structured to operate in a stable and predictable manner in response to any of the function or operating parameter configuration data.

21. The circuit chip of claim 1 which additionally comprises means responsive to an external control signal for simultaneously switching among a plurality of input signals to the chip and a corresponding plurality of sets of at least some of the configuration data, whereby the circuit chip is customized in its operation for the individual chip input signals.

22. The circuit chip of claim 1 which additionally comprises decoding circuitry receiving the configuration data and generating decoded binary signals coupled to circuit elements controllable thereby.

23. In an integrated circuit chip having a plurality of configurable circuit modules with programmable interconnections between them, a method of configuring the circuit chip into an operable system, comprising:

serially loading configuration data bits into the circuit chip by shifting a stream of said bits through serially arranged shift register stages,

transferring at least some of the configuration data bits in parallel from the shift registers into separate configuration registers, and

using the data bits in the configuration registers to obtain static signals that configure the circuit modules and program interconnections between them.

24. The method of claim 23 wherein the static signals are obtained by decoding individual fields of data bits stored in the configuration registers.

25. The method of claim 24 wherein data contained in one of at least two of said plurality of configuration registers are switchably selected for connection to at least one the decoders, thereby allowing a rapid change of the configuration data that is applied to at least some of the circuit elements.

26. The method of claim 24 wherein one of a plurality of input signals to the circuit chip is switchably selected simultaneously with the selection of of said at least two configuration registers for connection with said at least one of the decoders, thereby allowing the circuit chip configuration to be changed as the input signal is switched.

27. The method of claim 23, additionally comprising:

transferring the configuration data bits in parallel from at least some of the configuration registers into the shift registers, and

serially shifting the configuration data bits from the shift registers out of the circuit chip, thereby to unload the contents of said at least some of the configuration registers.

28. The method of claim 23 wherein individual ones of said series connected shift registers are addressed by controllably bypassing others of said shift registers.

29. The method of claim 23 wherein individual ones of said series connected shift registers providing configuration and/or interconnection data to one of the modules not being used is bypassed when shifting data through said series connected shift registers.

30. The method of any one of claims 23-29 wherein said plurality of configurable circuit modules are analog circuit modules.

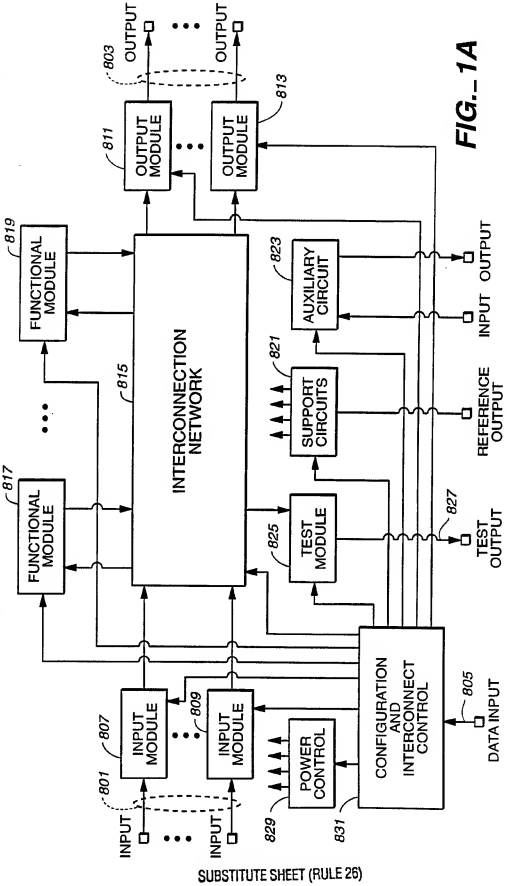
INPUT
INPUT
801
INPUT MODULE
807
INPUT MODULE
809
POWER CONTROL
829
CONFIGURATION AND INTERCONNECT CONTROL
831
805
DATA INPUT
FUNCTIONAL MODULE
817
FUNCTIONAL MODULE
819
INTERCONNECTION NETWORK
815
TEST MODULE
825
SUPPORT CIRCUITS
821
AUXILIARY CIRCUIT
823
827
TEST OUTPUT
REFERENCE OUTPUT
INPUT
OUTPUT
OUTPUT MODULE
811
OUTPUT MODULE
813
803
OUTPUT
OUTPUT

FIG._1A

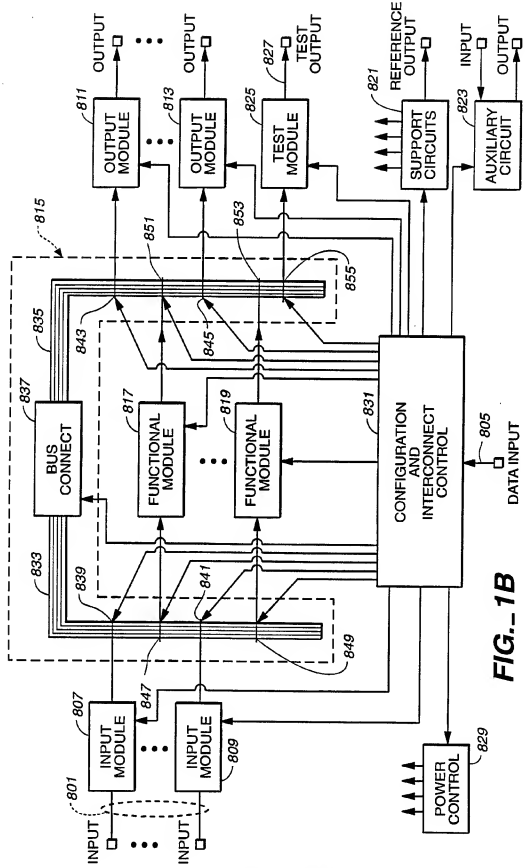
INPUT
INPUT
801
INPUT MODULE
807
INPUT MODULE
809
847
POWER CONTROL
829
815
OUTPUT MODULE
811
OUTPUT MODULE
813
TEST MODULE
825
827
TEST OUTPUT
OUTPUT
OUTPUT
SUPPORT CIRCUITS
821
REFERENCE OUTPUT
AUXILIARY CIRCUIT
823
INPUT
OUTPUT
851
853
855
835
843
845
837
BUS CONNECT
817
FUNCTIONAL MODULE
819
FUNCTIONAL MODULE
831
CONFIGURATION AND INTERCONNECT CONTROL
805
DATA INPUT
833
839
841
849

FIG._1B

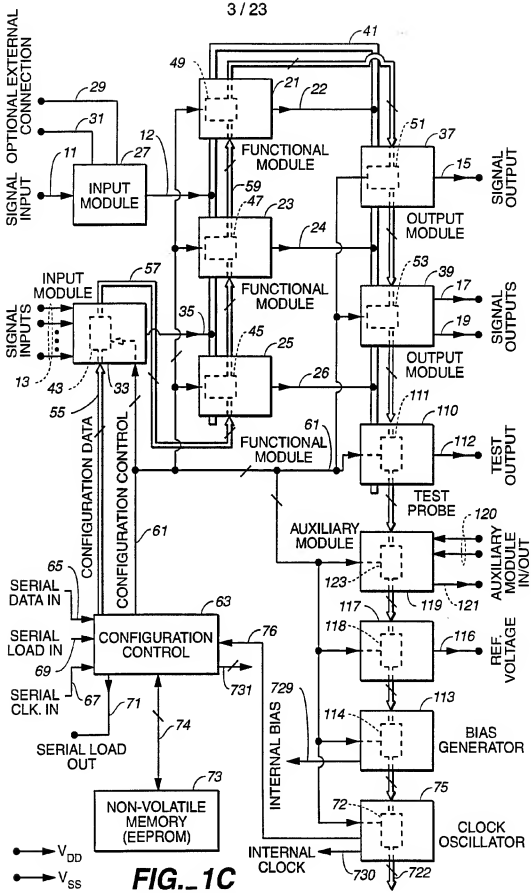
SIGNAL INPUT
OPTIONAL EXTERNAL CONNECTION
INPUT MODULE
FUNCTIONAL MODULE
OUTPUT MODULE
SIGNAL OUTPUT
SIGNAL INPUTS
SIGNAL OUTPUTS
TEST OUTPUT
TEST PROBE
AUXILIARY MODULE
AUXILIARY MODULE IN/OUT
REF. VOLTAGE
BIAS GENERATOR
CLOCK OSCILLATOR
CONFIGURATION DATA
CONFIGURATION CONTROL
SERIAL DATA IN
SERIAL LOAD IN
SERIAL CLK. IN
SERIAL LOAD OUT
NON-VOLATILE MEMORY (EEPROM)
INTERNAL BIAS
INTERNAL CLOCK
V_{DD}
V_{SS}

FIG._1C

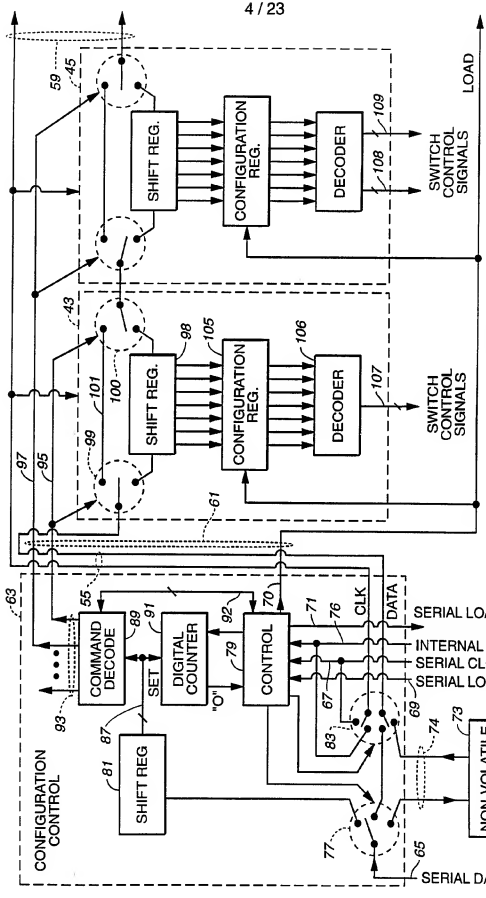
SHIFT REG.
CONFIGURATION REG.
DECODER
SWITCH CONTROL SIGNALS
LOAD
SHIFT REG.
CONFIGURATION REG.
DECODER
SWITCH CONTROL SIGNALS
COMMAND DECODE
DIGITAL COUNTER
CONTROL
SET
"0"
CLK
DATA
SERIAL LOAD OUT
INTERNAL CLOCK
SERIAL CLOCK IN
SERIAL LOAD IN
SERIAL DATA IN
SHIFT REG
NON-VOLATILE MEMORY
CONFIGURATION CONTROL

FIG._2

104
DATA BITS
103
NO. DATA BITS
85
COMMAND

FIG._3A

FIG._3B

INPUT MODULE 33
869
FUNCTIONAL MODULE 25
871
INPUT MODULE 27
873
881
INPUT AMP. GAIN
883
POWER
887
MUX
885
FILTER
889
AMP. GAIN
891
POWER
893
INPUTS AND POLARITY
895
BUS CONNECT
897
AMP. GAIN
899
POWER
901
FILTER AND EXTERNAL CONNECT
OUTPUT MODULE 37
875
AUXILIARY MODULE 119
877
903
VREF3
905
MODE
907
POWER
909
BUS CONNECT
879
CLK. OSC. 75

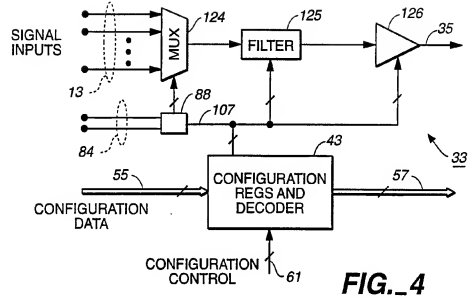
SIGNAL INPUTS
MUX
124
125
FILTER
126
35
13
88
107
84
43
33
55
CONFIGURATION REGS AND DECODER
57
CONFIGURATION DATA
CONFIGURATION CONTROL
61

FIG._4

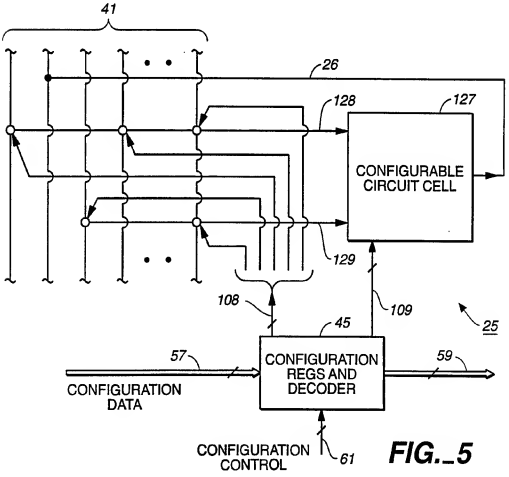
41
26
128
127
CONFIGURABLE CIRCUIT CELL
129
108
109
25
45
57
CONFIGURATION REGS AND DECODER
59
CONFIGURATION DATA
CONFIGURATION CONTROL
61

FIG._5

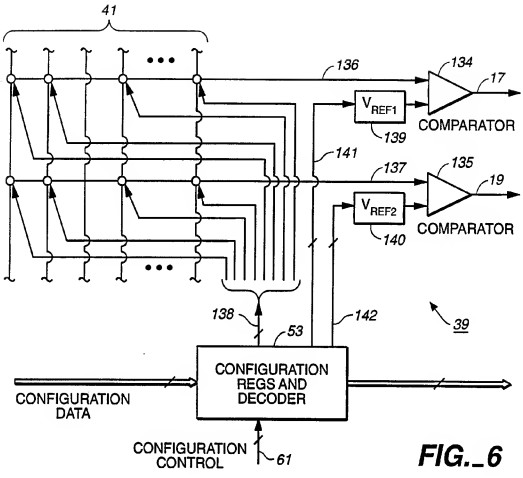
41
136
134
17
V_{REF1}
139
COMPARATOR
141
137
135
19
V_{REF2}
140
COMPARATOR
138
53
142
39
CONFIGURATION REGS AND DECODER
CONFIGURATION DATA
CONFIGURATION CONTROL
61

FIG._6

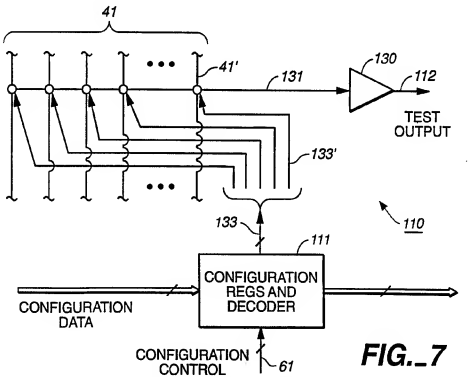
41
41'
131
130
112
TEST OUTPUT
133'
133
110
111
CONFIGURATION REGS AND DECODER
CONFIGURATION DATA
CONFIGURATION CONTROL
61

FIG._7

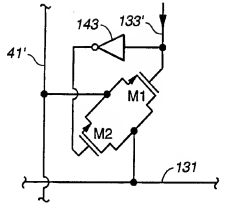

FIG._8

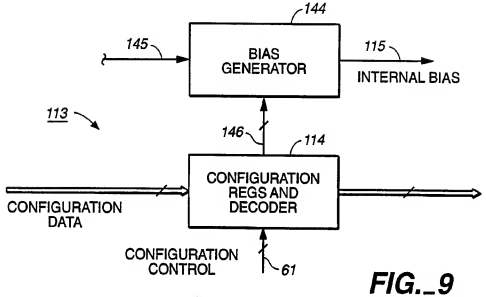

FIG._9

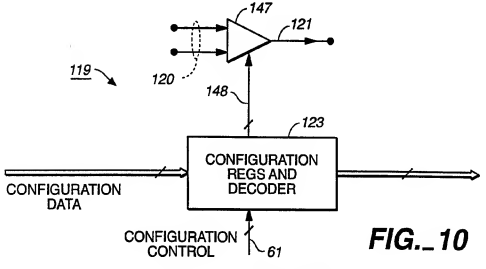

FIG._10

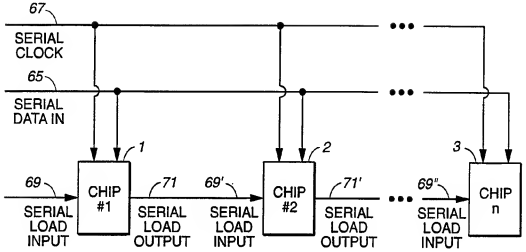

FIG._11A

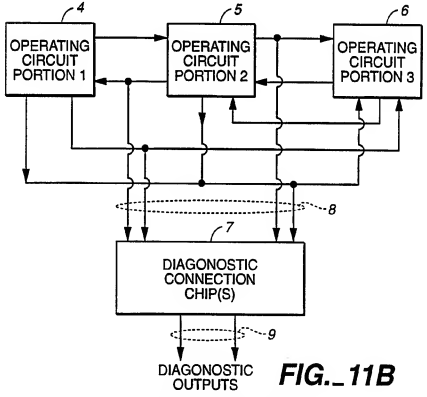

FIG._11B

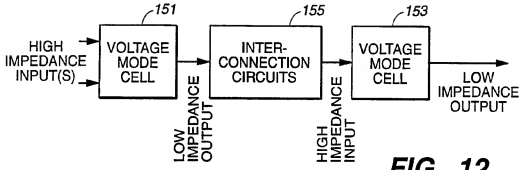

FIG._12

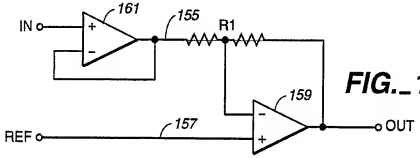

FIG._13a

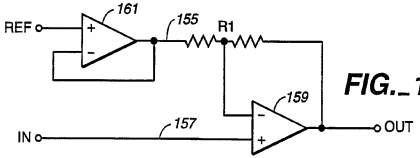

FIG._13b

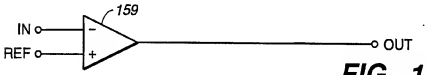

FIG._13c

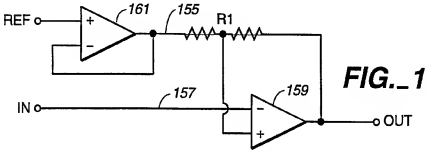

FIG._13d

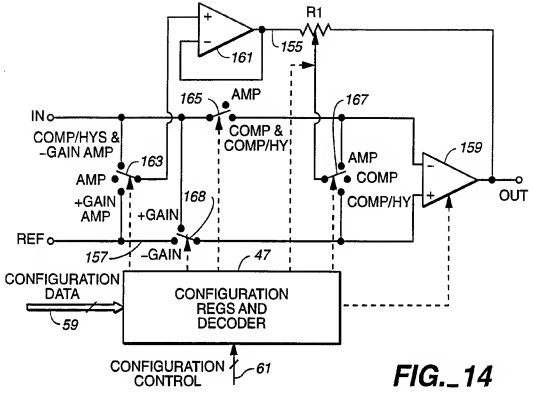
R1
155
161
165
AMP
167
IN
COMP/HYS &
-GAIN AMP
163
COMP &
COMP/HY
AMP
159
AMP
+GAIN
AMP
168
+GAIN
COMP
COMP/HY
OUT
REF
157
-GAIN
47
CONFIGURATION
DATA
59
CONFIGURATION
REGS AND
DECODER
CONFIGURATION
CONTROL
61

FIG._14

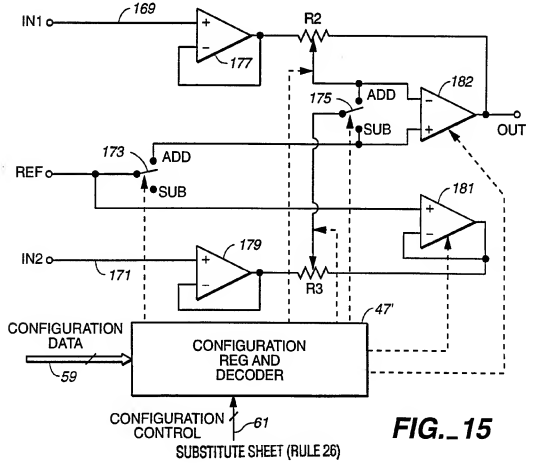
IN1
169
R2
177
182
175
ADD
SUB
OUT
173
ADD
REF
SUB
181
IN2
179
171
R3
47'
CONFIGURATION
DATA
59
CONFIGURATION
REG AND
DECODER
CONFIGURATION
CONTROL
61

FIG._15

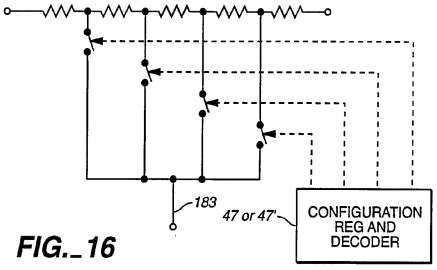

FIG._16

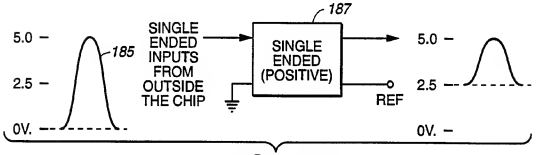

FIG._17a

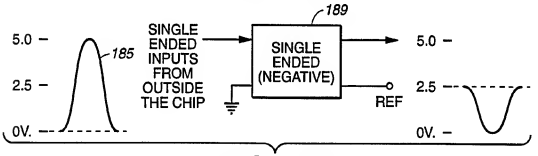

FIG._17b

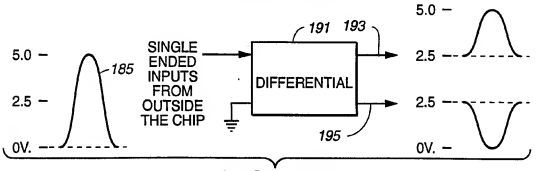

FIG._17c

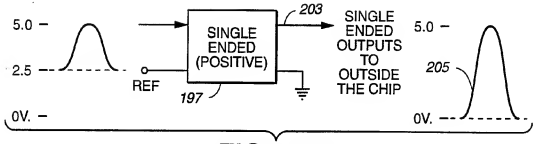

FIG._18a

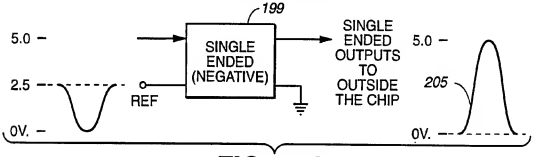

FIG._18b

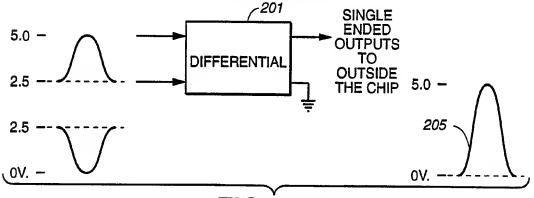

FIG._18c

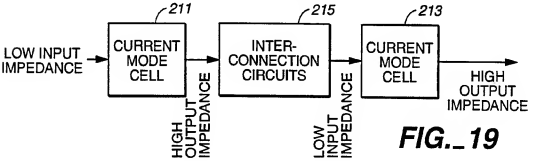

FIG._19

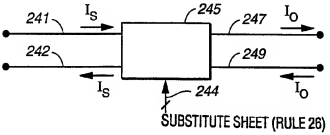

FIG._20

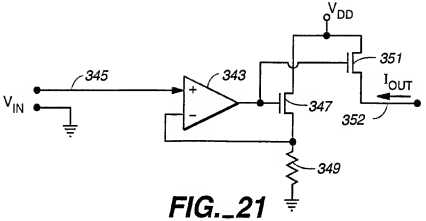

FIG._21

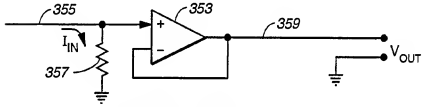

FIG._22a

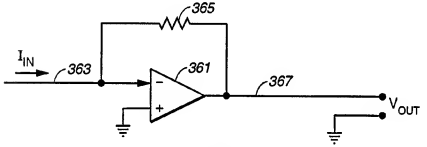

FIG._22b

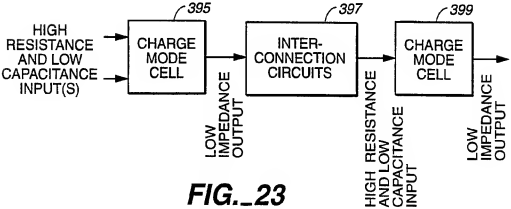

FIG._23

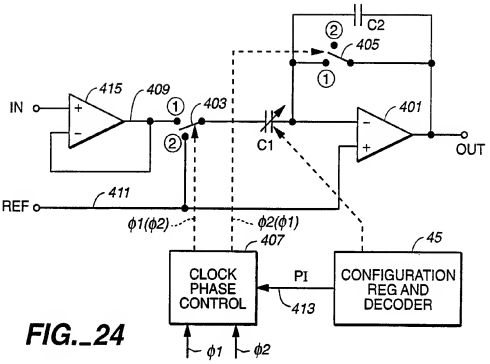
C2
405
415
409
403
401
IN
C1
OUT
411
REF
φ1(φ2)
φ2(φ1)
407
45
CLOCK PHASE CONTROL
PI
413
CONFIGURATION REG AND DECODER
φ1
φ2

FIG._24

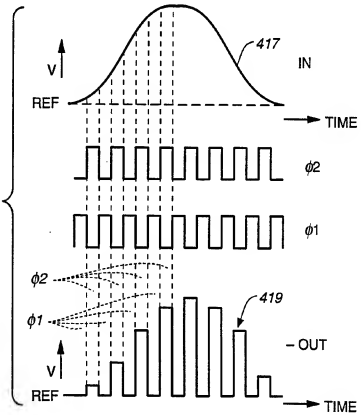
417
IN
V
REF
TIME
φ2
φ1
φ2
φ1
419
– OUT
V
REF
TIME

FIG._25

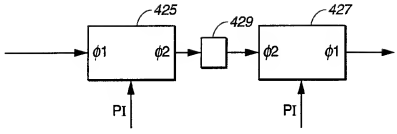
425
429
427
φ1
φ2
φ2
φ1
PI
PI

FIG._26

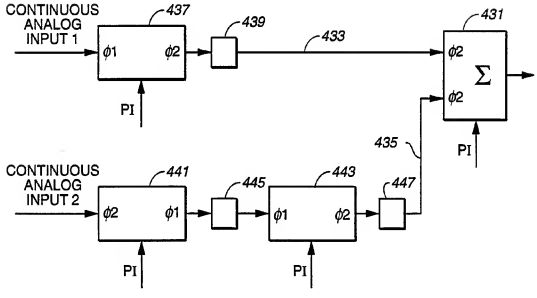
CONTINUOUS ANALOG INPUT 1
437
439
433
431
φ1
φ2
φ2
φ2
Σ
PI
PI
435
CONTINUOUS ANALOG INPUT 2
441
445
443
447
φ2
φ1
φ1
φ2
PI
PI

FIG._27

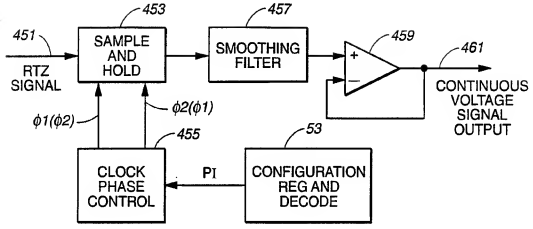
453
457
451
SAMPLE AND HOLD
SMOOTHING FILTER
459
461
RTZ SIGNAL
CONTINUOUS VOLTAGE SIGNAL OUTPUT
φ2(φ1)
φ1(φ2)
455
53
CLOCK PHASE CONTROL
PI
CONFIGURATION REG AND DECODE

FIG._28

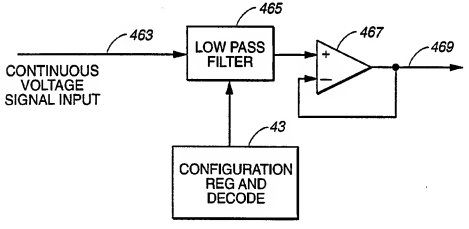
465
463
LOW PASS FILTER
467
469
CONTINUOUS VOLTAGE SIGNAL INPUT
43
CONFIGURATION REG AND DECODE

FIG._29

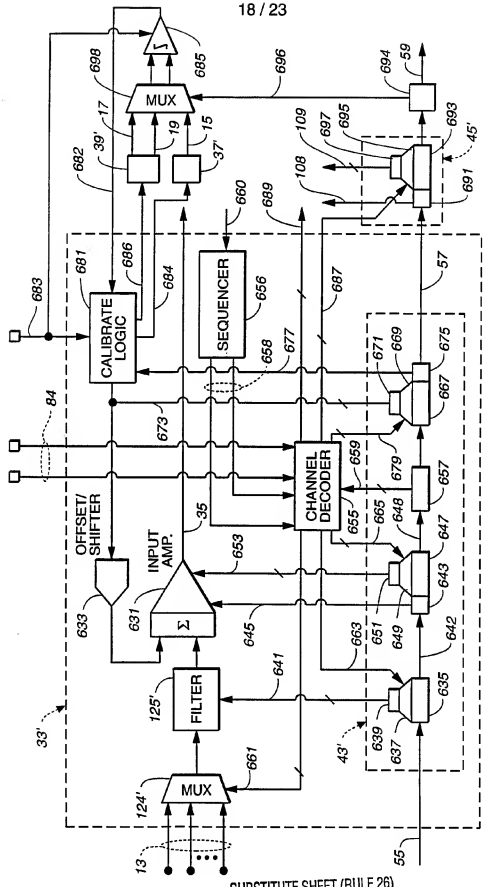
MUX
CALIBRATE LOGIC
SEQUENCER
CHANNEL DECODER
OFFSET/ SHIFTER
INPUT AMP.
Σ
FILTER
MUX
698
685
696
694
59
17
15
19
39'
37'
682
109
697
695
693
45'
108
689
691
660
681
686
684
656
687
57
683
677
658
671
669
675
667
84
673
659
679
657
655
665
648
647
35
653
643
633
631
645
649
651
663
642
641
635
125'
639
637
43'
33'
661
124'
13
55

FIG._30

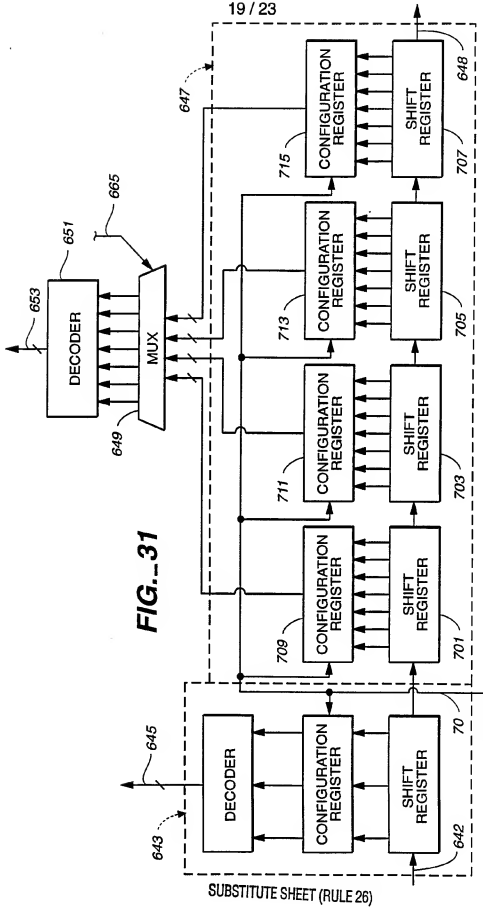
643
645
DECODER
CONFIGURATION REGISTER
SHIFT REGISTER
642
70
LOAD
647
651
665
653
DECODER
MUX
649
709
711
713
715
CONFIGURATION REGISTER
701
703
705
707
SHIFT REGISTER
648

FIG._31

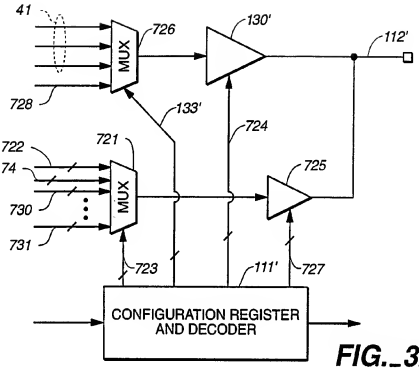
41
MUX
726
130'
112'
728
133'
724
722
721
74
MUX
725
730
731
723
111'
727
CONFIGURATION REGISTER AND DECODER

FIG._32

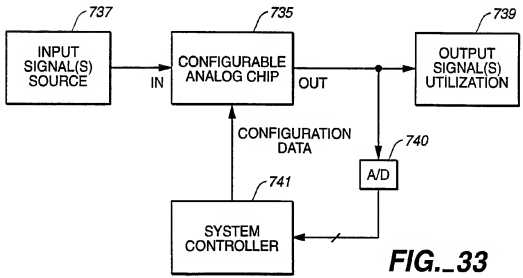
737
735
739
INPUT SIGNAL(S) SOURCE
IN
CONFIGURABLE ANALOG CHIP
OUT
OUTPUT SIGNAL(S) UTILIZATION
CONFIGURATION DATA
740
A/D
741
SYSTEM CONTROLLER

FIG._33

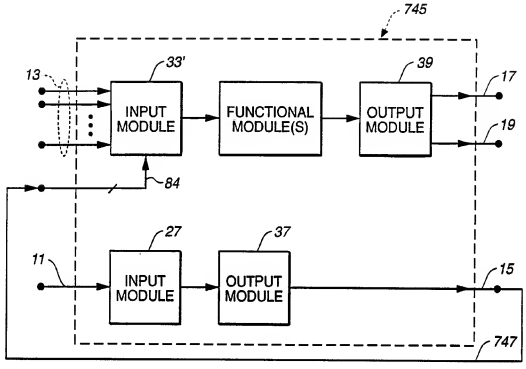
745
13
33'
INPUT MODULE
FUNCTIONAL MODULE(S)
39
OUTPUT MODULE
17
19
84
27
37
11
INPUT MODULE
OUTPUT MODULE
15
747

FIG._34

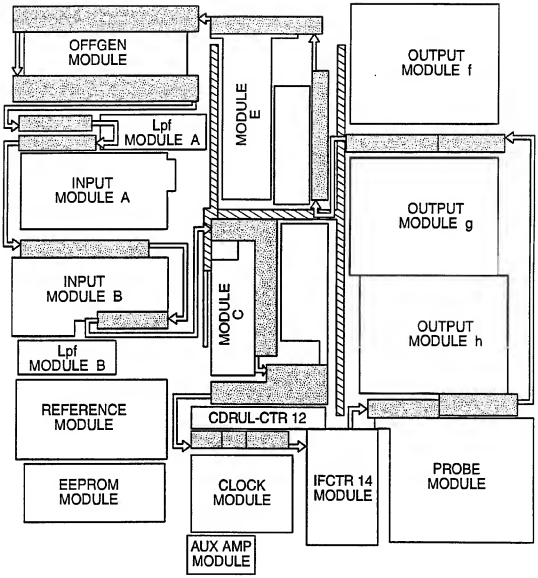
OFFGEN MODULE
Lpf MODULE A
INPUT MODULE A
INPUT MODULE B
Lpf MODULE B
REFERENCE MODULE
EEPROM MODULE
MODULE E
MODULE C
CDRUL-CTR 12
CLOCK MODULE
AUX AMP MODULE
IFCTR 14 MODULE
OUTPUT MODULE f
OUTPUT MODULE g
OUTPUT MODULE h
PROBE MODULE

FIG._35

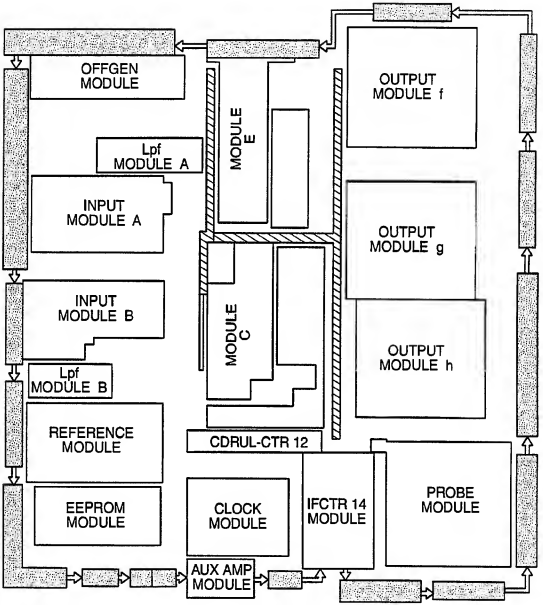
OFFGEN MODULE
Lpf MODULE A
INPUT MODULE A
INPUT MODULE B
Lpf MODULE B
REFERENCE MODULE
EEPROM MODULE
MODULE E
MODULE C
CDRUL-CTR 12
CLOCK MODULE
AUX AMP MODULE
IFCTR 14 MODULE
PROBE MODULE
OUTPUT MODULE f
OUTPUT MODULE g
OUTPUT MODULE h

FIG._36

INTERNATIONAL SEARCH REPORT

Intern. al Application No
PCT/US 95/06528

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06G7/06 G06J1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06G G06J G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP-A-0 450 863 (PILKINGTON MICRO-ELECTRONICS LTD) 9 October 1991	1-4,11, 12,14, 20,23, 24,30
Y	see column 1, line 31 - column 7, line 1; figure 1	5-7,9, 21,22, 25-27
Y	US-A-4 940 909 (MULDER ET AL.) 10 July 1990 see column 2, line 25 - line 68; figure 1	5-7,9, 21,22, 25-27

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 September 1995	12. 10. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Nielsen, O

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, vol. 34, 1 February 1991 pages 186-187, 314, XP 000238306 LEE E K F ET AL '1A CMOS FIELD-PROGRAMMABLE ANALOG ARRAY*' see the whole document ---	1,3,12, 14,15, 17-20, 23,24,30
X	US-A-5 245 262 (MOODY ET AL.) 14 September 1993 see column 1, line 66 - column 3, line 30; figure 3 ---	1,12,14, 16,20,21
X	ELECTRONICS LETTERS, vol. 28, no. 1, 1 January 1992 pages 28-29, XP 000278934 LEE E K F ET AL 'FIELD PROGRAMMABLE ANALOGUE ARRAY BASED ON MOSFET TRANSCONDUCTORS' see the whole document ---	1-3,14, 15,17, 19,20, 23,30
A	EP-A-0 322 382 (SGS-THOMSON MICROELECTRONICS S.R.L.) 28 June 1989 see page 2, line 32 - page 3, line 43 see page 4, line 52 - line 57 ---	1
P,X	ELECTRONIC DESIGN, vol. 42, no. 21, 14 October 1994 page 63/64, 66, 68, 70/71, 73 XP 000477345 GOODENOUGH F 'ANALOG CONTERPARTS OF FPGAS EASE SYSTEM DESIGN' see the whole document -----	1-30

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inl ational Application No
PCT/US 95/06528

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-450863	09-10-91	AU-B-	639543	29-07-93
		AU-A-	7405191	10-10-91
		CN-A,B	1055436	16-10-91
		EP-A-	0450866	09-10-91
		GB-A,B	2242801	09-10-91
		GB-A,B	2246666	05-02-92
		JP-A-	5175466	13-07-93
		JP-A-	5145038	11-06-93
		US-A-	5196740	23-03-93
US-A-4940909	10-07-90	NONE		
US-A-5245262	14-09-93	NONE		
EP-A-322382	28-06-89	DE-D-	3851423	13-10-94
		DE-T-	3851423	19-01-95
		JP-A-	2004001	09-01-90
		US-A-	4875020	17-10-89